PCI Express® 4.0 CEM TX Signal Quality Testing for Keysight UXR-Series, Z-Series, V-Series, or equivalent Real-Time Oscilloscopes

Version 0.7

Revision History

Version	Date	Summary of Changes	Contributor(s)
0.7	1.16.2019	Initial Draft PCIe 4 TX Preset, TX Signal Quality, PWJ Testing	Rick Eads

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Overview

This document contains the procedure for testing PCI Express 4.0 CEM based endpoint and root complex devices that support 16GT/s using Keysight real time oscilloscopes including the UXR-Series, Z-Series, V-Series, Q-Series, X-Series or other equivalent Keysight oscilloscope having a minimum bandwidth of 25GHz. For the purposes of this document, Keysight "real-edge" channels capable of bandwidth above 33GHz are not included in this test procedure.

This document provides details on:

1. Measuring the correct transmitter equalization values for each preset and verifying that the specified transmitter equalization values meets eye diagram and other jitter requirements using the PCISIG's PCIe 4.0 Compliance Test Fixtures (CBB4, CLB4, and Variable ISI Channel) at speeds of 16GT/s.

2. Analyzing the data used to test the endpoint or root complex device against the PCIe 4.0 CEM specification is done using SigTest version 4.0.45 or later.

Note:The tests described in this document are intended to provide information about the tests that will be used in PCI-SIG compliance program. This testing is not a replacement for an exhaustive test validation plan. Also, all content in this test procedure is subject to change without notice.

Please read through this entire document before you proceed with testing your endpoint or root complex device so that you may become familiar with the overall testing procedure.

Please refer to the following documents on www.pcisig.com for more specific information related to the PCI Express 4.0 specification.

- PCI Express® Base Specification Revision 4.0, Ver. 1.0
- PCI Express® Card Electromechanical Specification Revision 4.0, Ver. 0.9

1. **Oscilloscope:** This document was developed using Keysight digital storage oscilloscope, Model# UXR0334A having a bandwidth of 33 GHz. This scope gives a maximum sampling rate of 128GS/s on four channels simultaneously and up to 2G of acquisition memory. References to other Keysight Oscilloscopes such as the Z-Series, V-Series, Q-Series and X-Series are also implied by any reference to the V-Series as all share the same user interface for the testing purposes describe in this document.

Figure 1 Keysight UXR Series 33GHz, 4-channel, real time oscilloscope

2. Cables:
   a) 2.92mm(m)-2.92mm(m) phase matched cable pair ~ 1m in lenght, Huber+Suhner. Qty=2 pairs for root complex testing, qty=1 pair for endpoint testing. NOTE: It is recommended cables pairs be phase matched to 1ps. These must be ordered separately. (Use Huber+Suhner PN: 85104455 or PCI SF126E/11PC35/11PC35/914mm)

   b) Short SMP (female) to 2.92mm (female) connectors (supplied with CEM 4.0 test fixture kit)
   Qty = 2 for Add In Card testing, Qty = 4 for System testing

   c) SMP (female) to SMP (female) connector cable assembly (supplied with CEM 4.0 test fixture kit), 1 foot long. Qty = 1 matched pair (2 total)

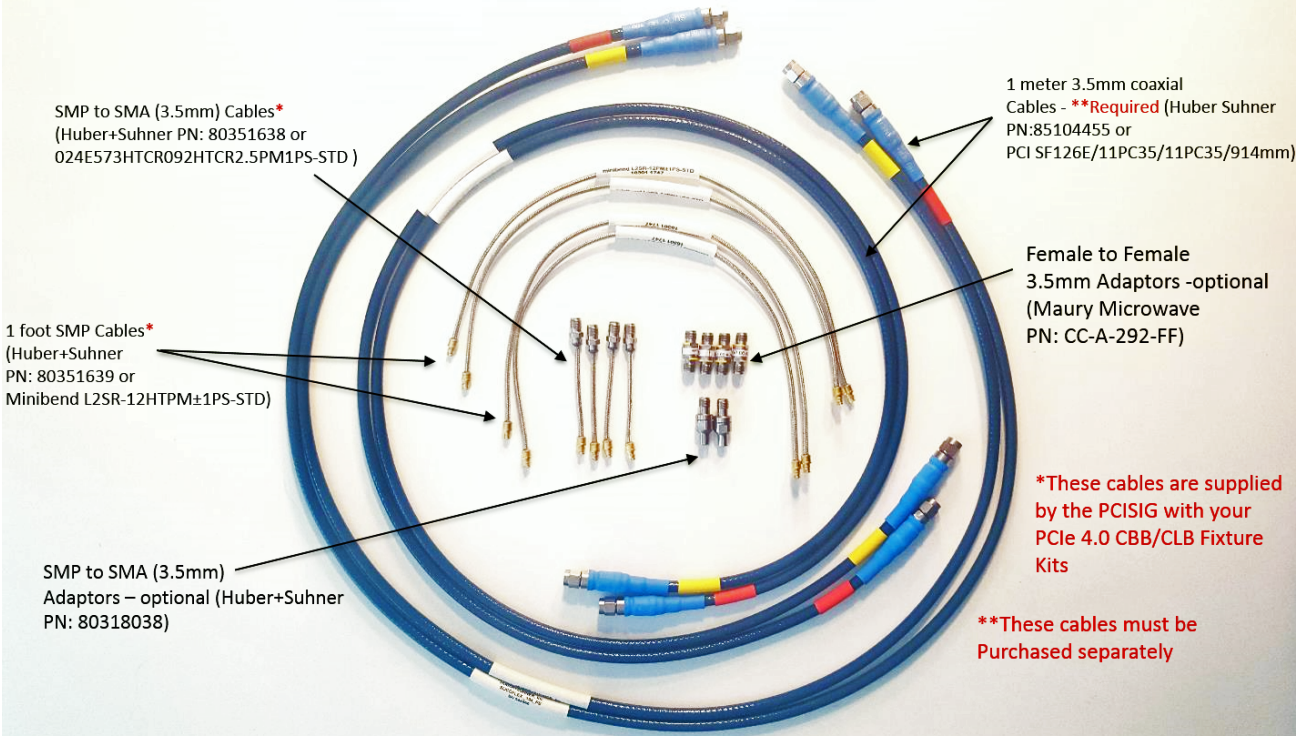


Figure 2 Cables, adapters and accessories for PCIe 4.0 testing

3. **Accessories**
   Terminators (SMP, male, 50-ohm, Fairview Microwave PN/ST1847, qty=30)
   ATX Power Supply with 24-pin connector for add-in cards (qty=1)

4. **Probes**
   In the case where you are doing root complex (motherboard) tests with a two-channel oscilloscope with a minimum bandwidth of 25GHz, you can use two of the N2802A active probes with two N5444A Differential 3.5mm (SMA compatible) probe heads. This allows you to measure one differential high speed data signal and the differential system clock simultaneously.

Figure 3 Differential probe heads can be substituted for direct cable connections which is useful for dual-port, motherboard tests when using oscilloscopes with two channels.

5. **Test Fixtures**
   Revision 4.0 Compliance Base Board (CBB), Compliance Load Board (CLB), & variable ISI board

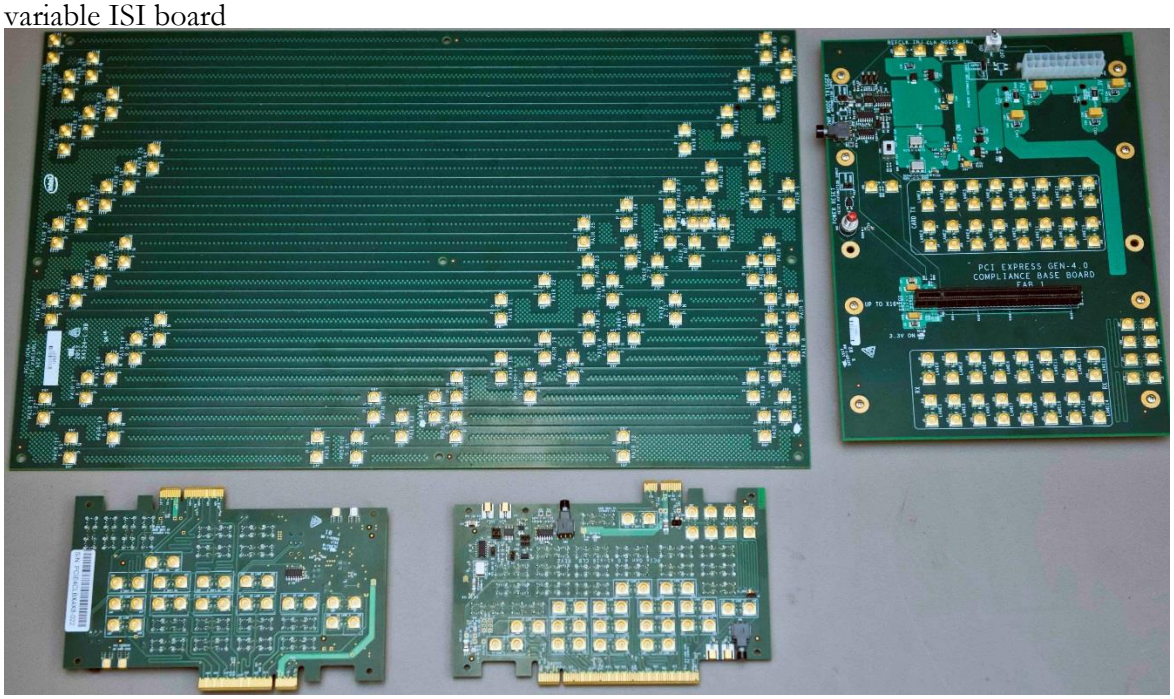


Figure 4 PCIe 4.0 CEM compliance fixtures consist of two CLBs (a x4/x8 and a x1/x16 board), one CBB and a variable ISI channel board

The compliance fixtures required for testing include a CBB for endpoint testing and two CLBs for root complex testing that support x1, x4, x8, or x16 CEM slot widths on the root complex device. Test fixtures are available from the PCI-SIG at http://pcisig.com/specifications/order-form.

Software Requirements

1. SigTest
   PCI Express 4.0 TX Compliance is measured using the PCI-SIG's SigTest tool. This tool can be downloaded from Intel at: http://www.intel.com/high-speed-io. This document was written using SigTest 4.0.45 for testing at 16GT/s

2. PCIe 4.0 at lower data rates
   For testing PCIe at lower data rates of 2.5G, 5G, and 8GT/s, use SigTest 3.2.0.3 and follow the test procedures written for testing PCI Express 3.0. This version of SigTest can be downloaded from the same located noted above. This document focuses only on testing 16GT/s. For TX Testing only (not RX testing), it is acceptable to use the PCIe 4.0 CEM test fixtures to test the lower data rates.

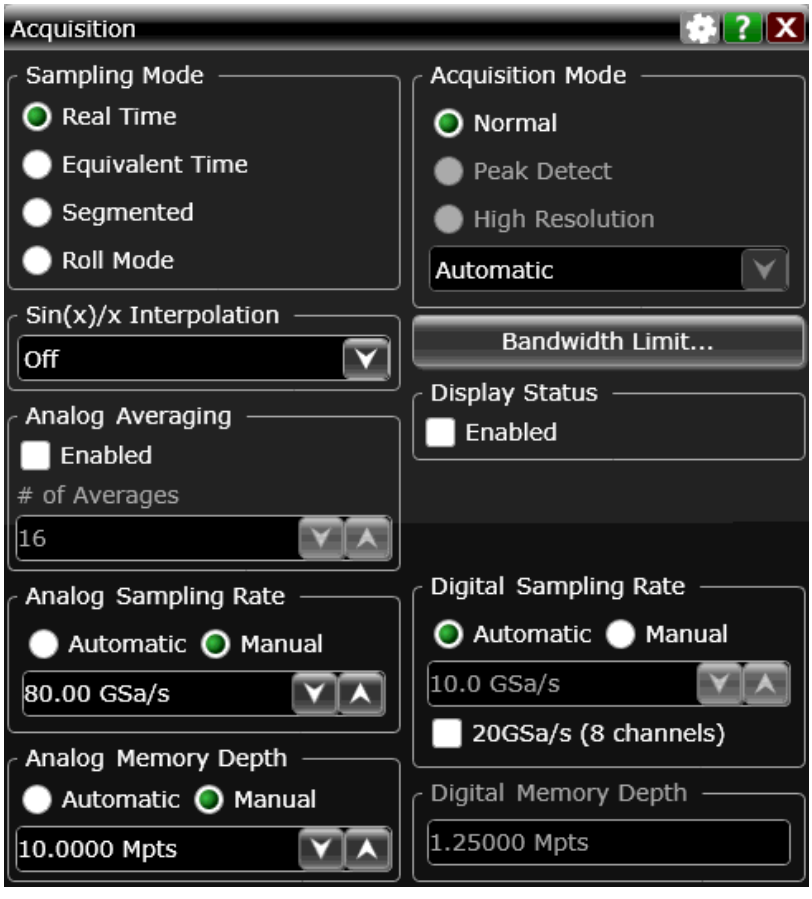
Oscilloscope Setup

For all TX measurements of your PCIe 4.0 device you need to setup your oscilloscope to be able to capture the waveforms with enough depth and bandwidth to ensure good signal integrity. This section reviews some basic setup procedures for ensuring your signals are properly scaled, that your bandwidth is set correctly, and that your memory depth and channel setup is optimized for making PCIe 4.0 measurements.

It is assumed that you are already working with an oscilloscope that has been properly calibrated and that the cables you are using have also been calibrated and the oscilloscope channels have been deskewed. Refer to the PCIe 3.0 test procedures to review how this is done if needed. (Refer to the next section for CBB4 Setup)

1. It is usually a good practice to start any instrument configuration process by initializing the instrument to a consistent state. For convenience, you may want to press the **Default Setup** on the front panel of the oscilloscope before you begin.

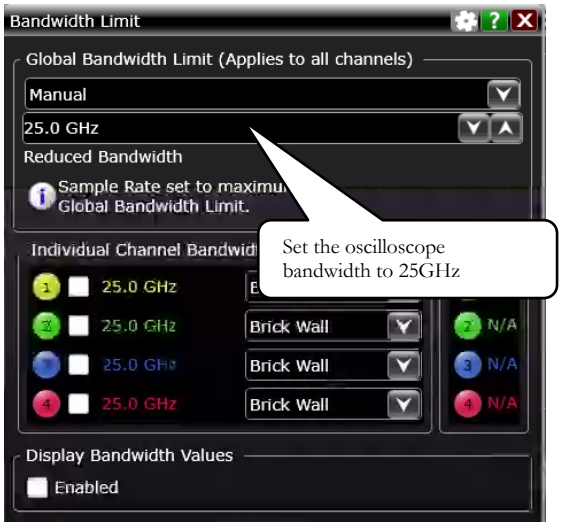
2. Configuring the acquisition and oscilloscope memory.
   a) For PCIe 4.0 the minimum oscilloscope bandwidth required is 25GHz. To set this bandwidth, select **Setup -> Acquisition** from the drop-down menu.



   b) On this page you want to do a number of things:
      a. Turn Sin(x)/x Interpolation off
      b. Set the sample rate to the maximum (manually). In this case we are using 80GSa/s but it could be different depending upon your particular oscilloscope.

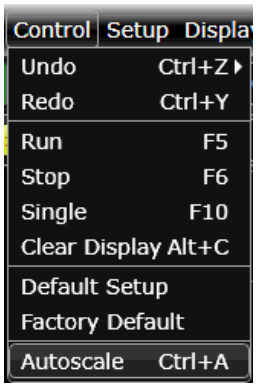
c. Set the memory depth appropriate to capture 2M UI. With 80GSa/s we need to set the memory depth to 10M points. Depending on the scope you are using, the actual number of points you need to capture 2M UI could be different.

d. Next select the **Bandwidth Limit** button and set the oscilloscope bandwidth to 25GHz on all channels.



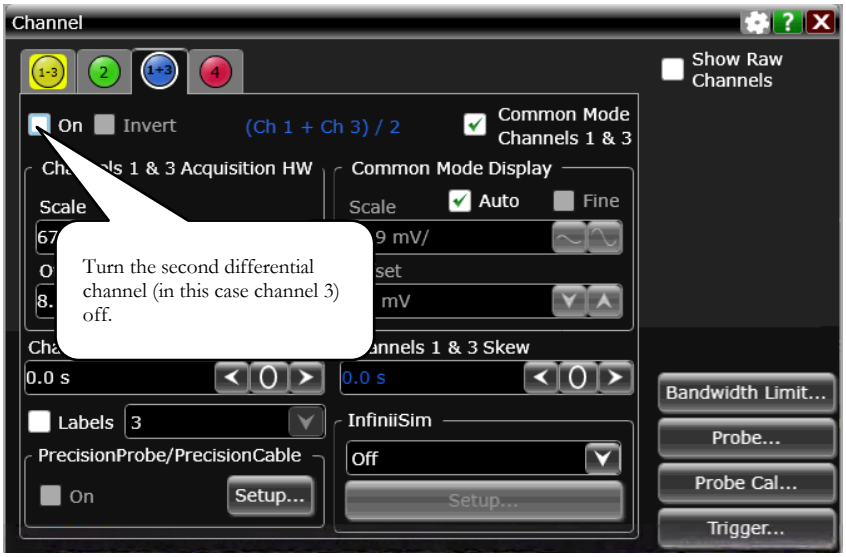
3. Autoscaling the signal

a) Once you have connected your 16GT/s signal to the oscilloscope and your DUT is transmitting P0 at the proper level of de-emphasis, you want to be sure that the oscilloscope's dynamic range is optimized for the amplitude of the signal. To do this you turn on the channels for each of the differential signals (D+, D-, and CLK+, CLK- if appropriate) you plan to capture. Then select **Control -> Autoscale** from the drop-down menu.

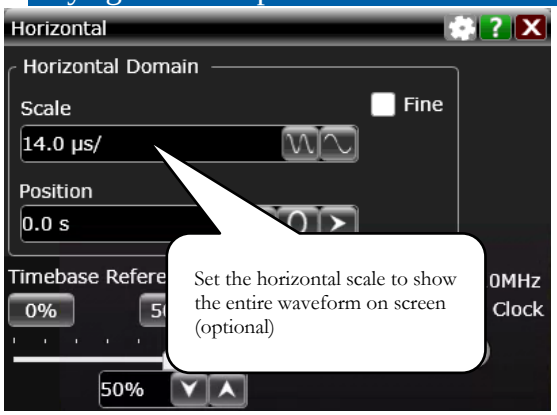


b) With both channels of the differential signal now properly scaled, you want to setup a hardware differential channel by selecting **Setup -> Channel 1** from the drop-down menu.

c) Since now both differential signals have been combined into one combined signal in hardware, you can now turn off the second differential signal (it is now showing the common mode of the differential channel). To do this you select the second channel (in this case it is Channel 3) on the Channel screen and then you turn it off.



d) Now set the scale so that the entire waveform is on-screen. This is for your convenience and may help ensure that you are able to save all of the waveforms with the proper number of unit intervals in your data files. Use the drop-down menu Setup -> Horizontal to enter this selection. For the scope in this example, 14us/division was used as shown.



e) You should see a screen that looks something like this: (P0 at 16GT/s is displayed).

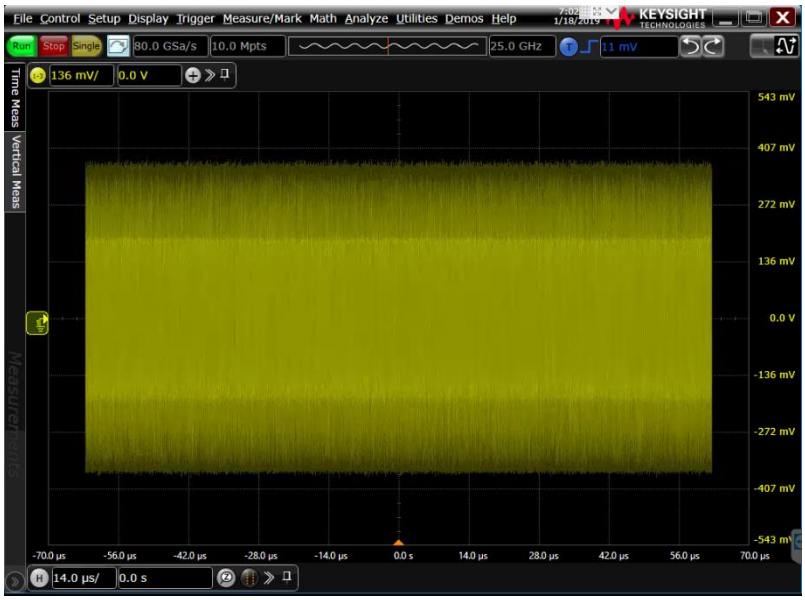
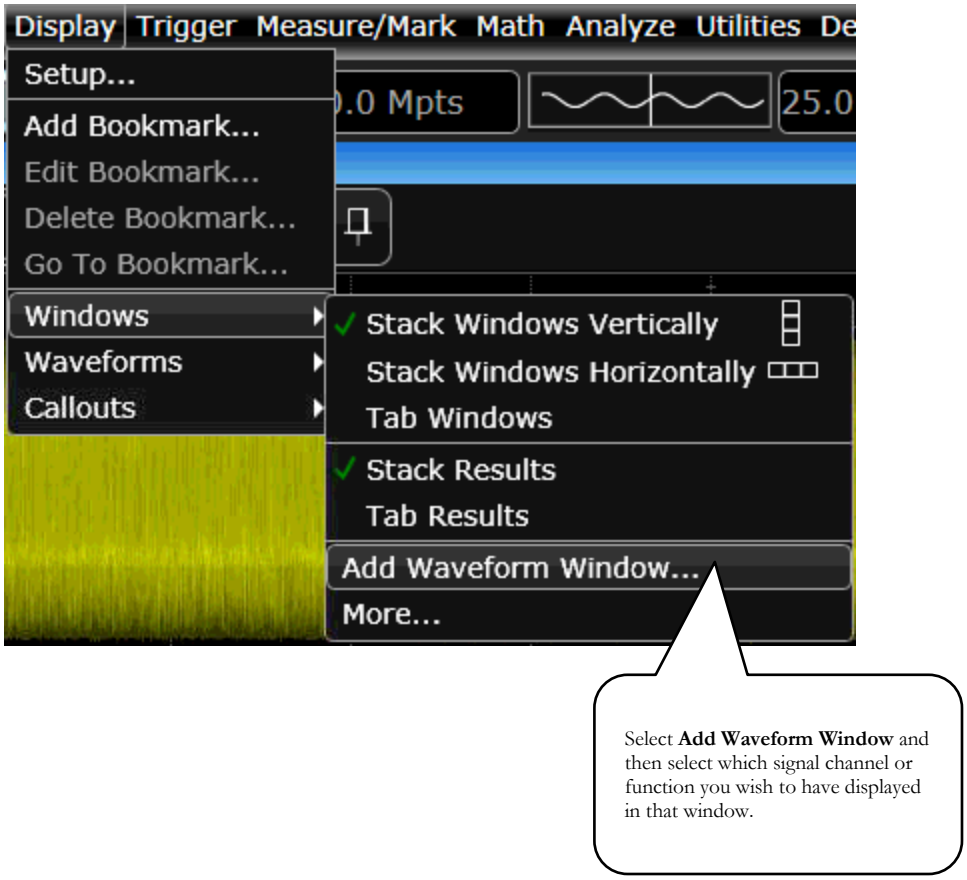


Figure 5 A properly scaled and configured PCIe 4.0 Signal from and endpoint device ready to be analyzed.

4. Additional instructions for setting up root complex waveform captures. Setting up the capture of a root complex data signal is very much identical to setting up the data signal for an endpoint device. Here are a few additional items to keep in mind.
   a) For root complex CEM testing you need to include the capture of the reference clock. This requires that you have:
      a. An oscilloscope that is capable of 25GHz on 4 channels like the Keysight UXR or Z-Series oscilloscopes.
      b. Or, use active probes on a V-Series or UXR 2-Channel scope (some 40GHz and above models) that allows you to probe two differential signals with only two channels.
   b) Once you have both the data and clock signals connected to the oscilloscope you scale and configure hardware differential channels for both. For example, assume you have the 16GT/s channels connected with D+ on Channel 1 and D- on Channel 3. The HW differential channel will be configured for CH1-3. Likewise, the differential root complex common clock will be connected to Channel 2 and Channel 4. Once properly scaled, the clock will utilize hardware differential channel CH2-4. In this example only CH1-3 and CH2-4 will be enabled (turned on).

c) TIP: you can create a second waveform window for the CLK signal with the command from the drop-down menu **Display -> Windows -> Add Waveform Window**.



The nomenclature "[PHY 2.x]" refers to the section of the PCI Express Architecture PHY Test Specification Rev 4.0 and designates the, numbered test assertion in that document.

[PHY 2.3] Add-in Card Transmitter Preset Test for 16GT/s

This procedure determines whether the device under test produces the correct TX transmitter equalization for each of the eleven (P0-P10) presets. Lanes which are not being tested should be terminated with 50-ohm terminations. You will also use this setup to capture a toggle pattern (with crosstalk)

5. Configure the CBB4 as shown below. This setup is used for both Preset Testing

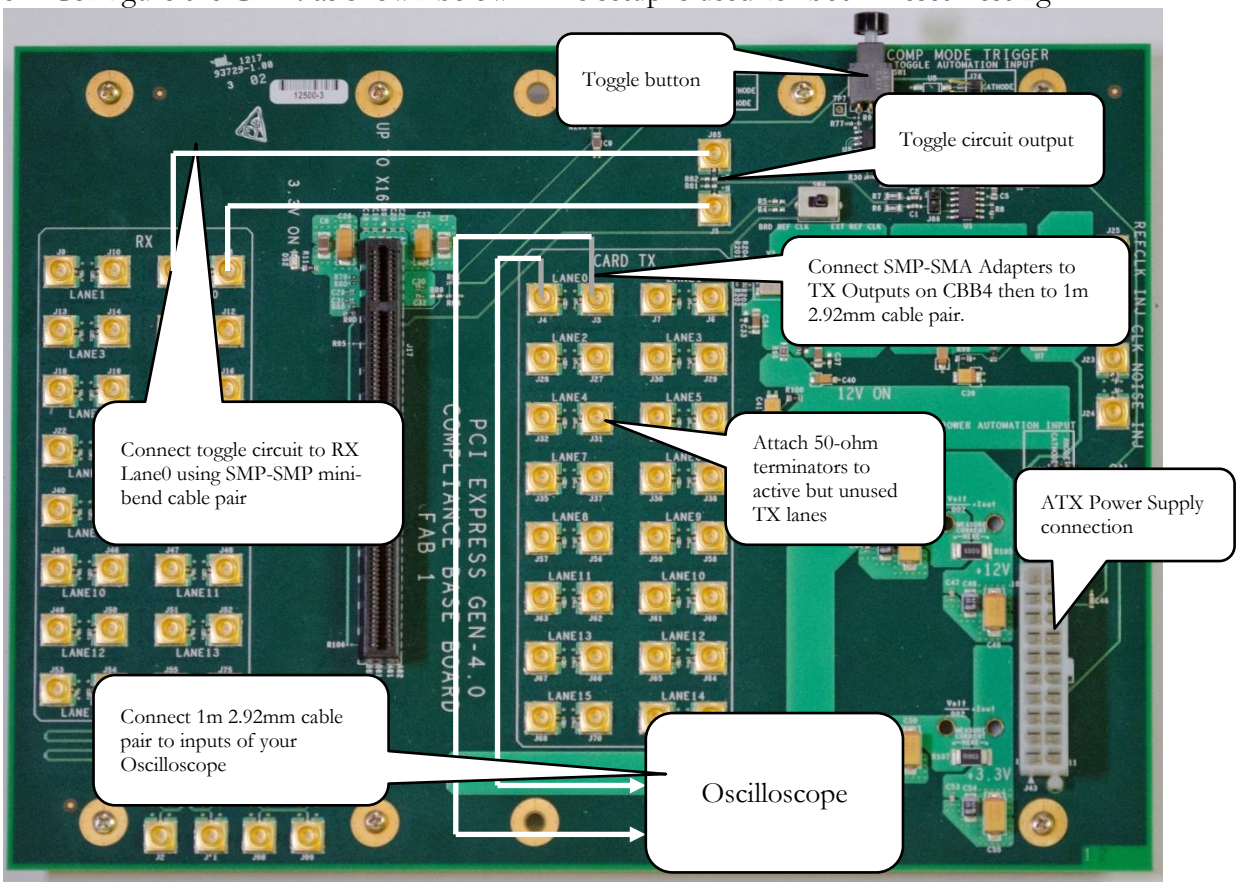
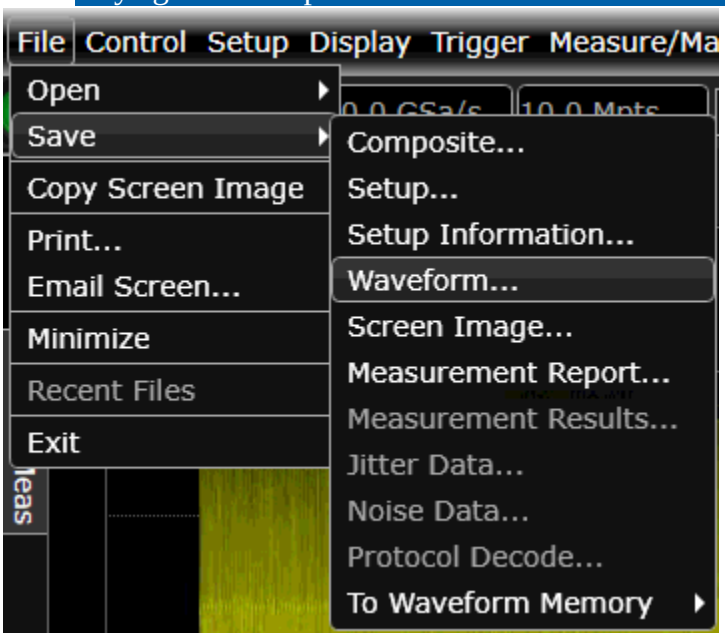
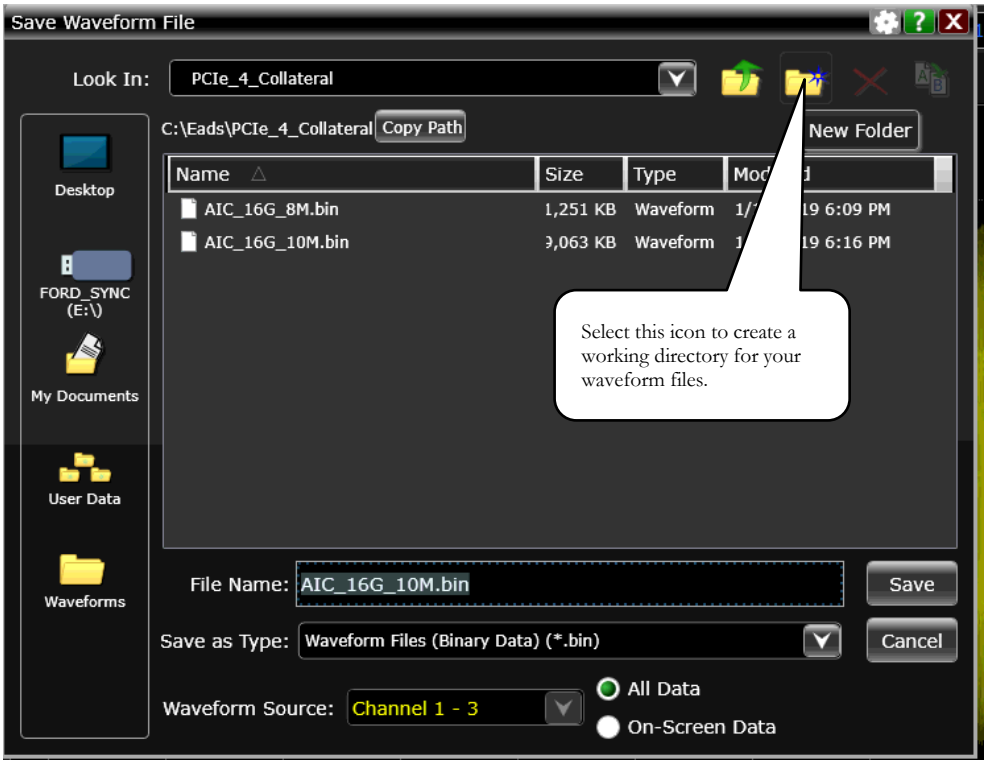


Figure 6 Add-in card connection diagram for PCIe 4.0 endpoint transmitter (TX) testing of TX Presets

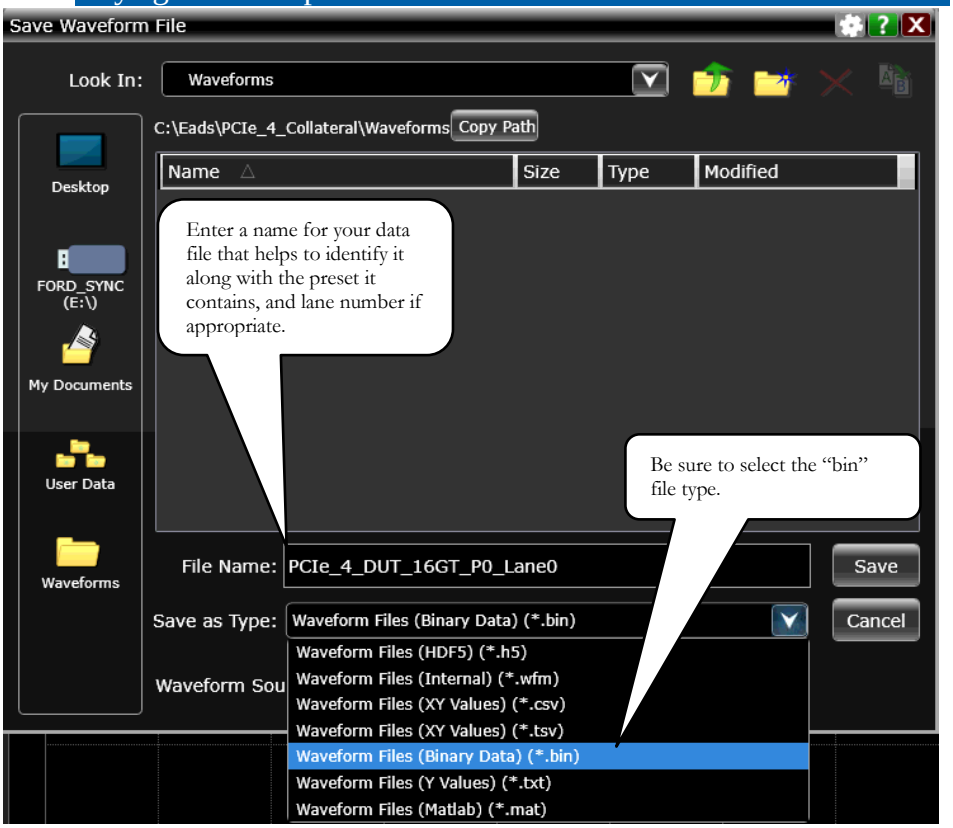
6. Assuming your oscilloscope is properly setup and is currently displaying P0 at 16GT/s and is properly scaled and configured, these are the next steps to capturing and analyzing the presets P0-P10. First you will want to setup a location in which you can store your data. Select File -> Save -> Waveform to open the file management dialog page.



7. Then select the new folder icon in order to create a new folder in your directory of choice.



8. When you have selected your directory, then pick an appropriate name for your data file and save that file as a "**Type Waveform Files (Binary Data (*.bin)**"



9. Next, using the toggle button on the CBB4, cycle through all of the DUT presets P1-P10 and repeat the above process to save a file for each of the 11 presets.

   TIP: Using the naming convention described by the *Gen3_Preset_Instructions.docx* file included with the SigTest 4.0.45 installation, SigTest is able to automatically input and analyze all of the preset files in a given container folder. The file name should contain a substring of the form _Pnn_t_ where 'nn' is the preset number between 00 and 10 and 't' is the type of the waveform: 'd' for differential, For example, "TID1001_Ln00_P04_d_16GT.bin" indicates a differential measurement of preset 4.

10. After you have captured Preset P10, press the toggle button two more times and you should see a toggle pattern (101010 repeating). Capture this waveform to an appropriate file name. You will use this later while post processing your data to determine your pulse width jitter.

11. Refer now to the section in this document entitled "Data Post Processing" for instructions on how to analyze the data you have captured

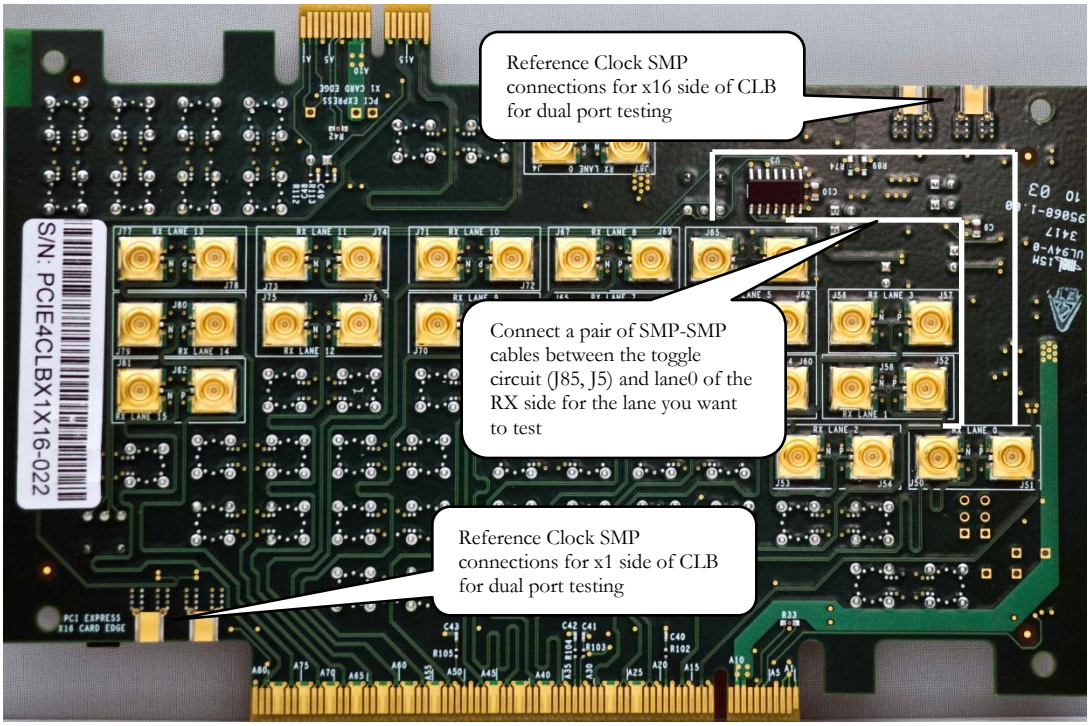
[PHY 2.8] System Board Transmitter Preset Test for 16GT/s

This section of the test procedure shows how to measure the system board or root complex transmitter to determine whether or not the proper levels of de-emphasis are being generated for each of the 11 presets P0-P11 at 16GT/s.

1. There are two Compliance Load Boards in the PCIe 4.0 CEM fixture kit. Choose the load board appropriate for the lane width of the slot you plan to test (either x1, x4, x8, or x16). For unused lanes, be sure to terminate them appropriately with SMP 50-ohm terminators. Note each board has an RX and TX side.

Figure 7 CLB4 Fixtures for x1, x16 and x4, x8 testing

2. Once you determine the lane width of the CEM connector interface on your system board that you want to test, configure the appropriate CLB4 as shown in the example below. This photo shows the connection necessary to use the CLB toggle function to force the DUT to switch between the TX compliance patterns.



3. On the TX side of the CLB4, connect the SMP-SMA short cables to the 2.92mm, 1m cables and then connect those cables to the lane that you want to test.

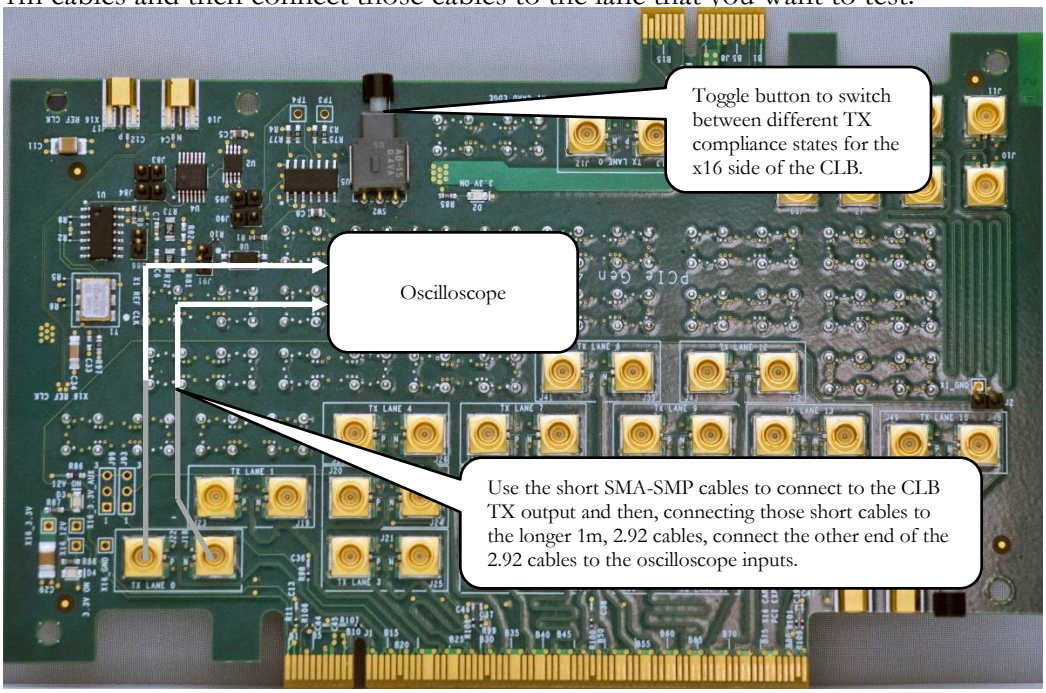
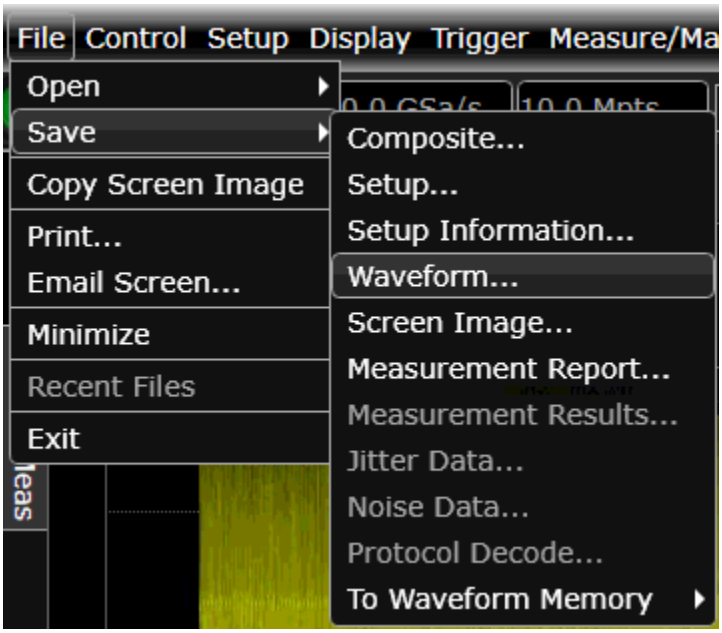
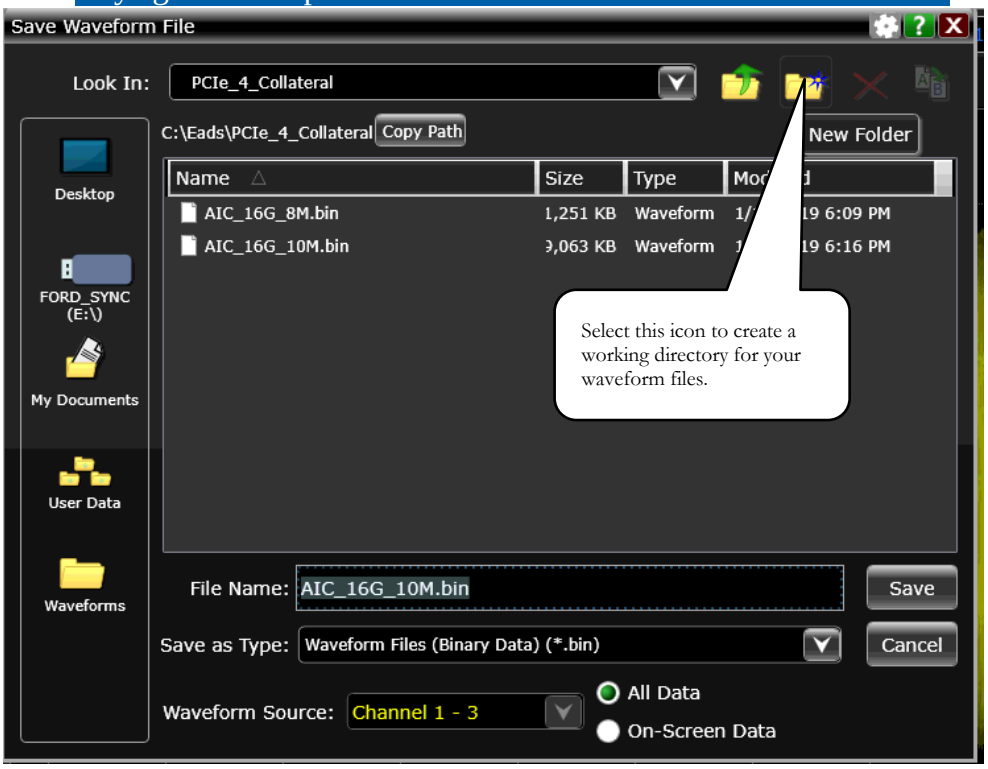


Figure 8 System board connection diagram for PCIe 4.0 transmitter (TX) testing of TX Presets

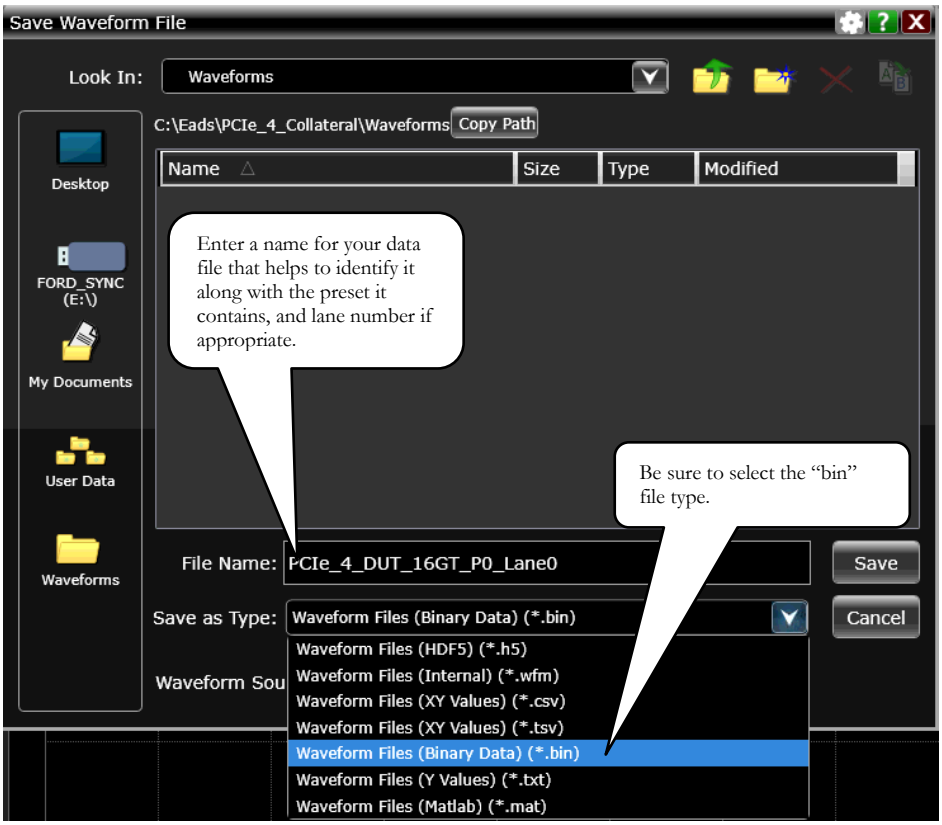
4. Assuming your oscilloscope is properly setup and is currently displaying P0 at 16GT/s and is properly scaled and configured, these are the next steps to capturing and analyzing the presets P0-P10. First you will want to setup a location in which you can store your data. Select File -> Save -> Waveform to open the file management dialog page.



5. Then select the new folder icon in order to create a new folder in your directory of choice.



6. When you have selected your directory, then pick an appropriate name for your data file and save that file as a "**Type Waveform Files (Binary Data (*.bin)**"



7. Next, using the toggle button on the CBB4, cycle through all of the DUT presets

P1-P10 and repeat the above process to save a file for each of the 11 presets.

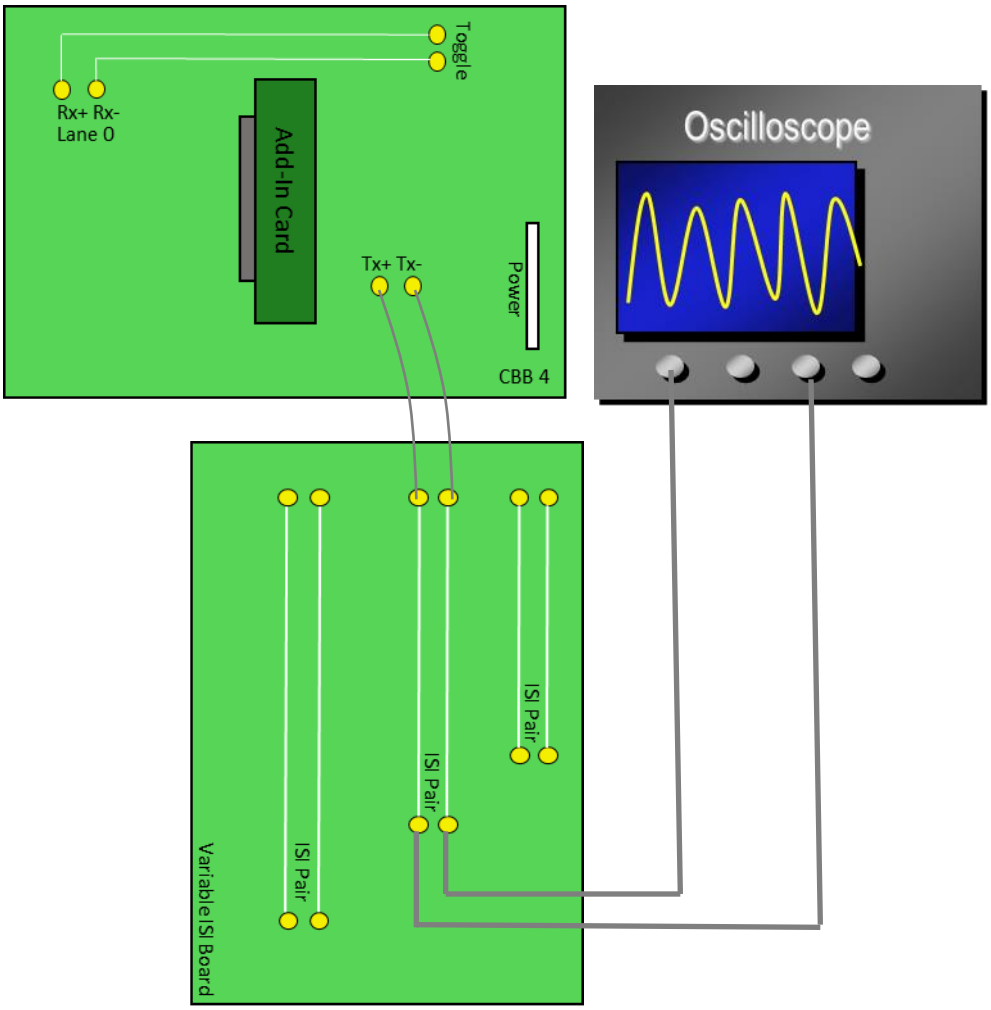
TIP: Using the naming convention described by the *Gen3_Preset_Instructions.docx* file included with the SigTest 4.0.45 installation, SigTest is able to automatically input and analyze all of the preset files in a given container folder. The file name should contain a substring of the form _Pnn_t_ where 'nn' is the preset number between 00 and 10 and 't' is the type of the waveform: 'd' for differential, For example, "TID1001_Ln00_P04_d_16GT.bin" indicates a differential measurement of preset 4.

8. Refer now to the section in this document entitled "Data Post Processing" for instructions on how to analyze the data you have captured

[PHY 2.1] Add-in Card Transmitter Signal Quality Test for 16GT/s.

This section of the test procedure verifies that the signaling of the add-in card device meets the eye diagram and other requirements. Lanes that are not being tested should be terminated with 50-ohm SMP terminators.

1. Configure the measurement connection setup as indicated below. Note that this is an end-of-channel test and as such requires that you emulate the maximum allowable channel loss as per the PCIe 4.0 CEM connection. The particular ISI pair that you use for this setup is determined by a number of factors including the loss of your cables, your particular CEM fixture, and adapters. For more detail on characterizing your fixtures and cables, please refer to the 2018 US Devcon presentation entitled, "PCIe® 4.0 Electrical Compliance Testing Deep Dive". Assuming you are using the recommended cables listed in the beginning of this document, we will assume "pair 16" has the appropriate amount of loss but you should verify this independently.

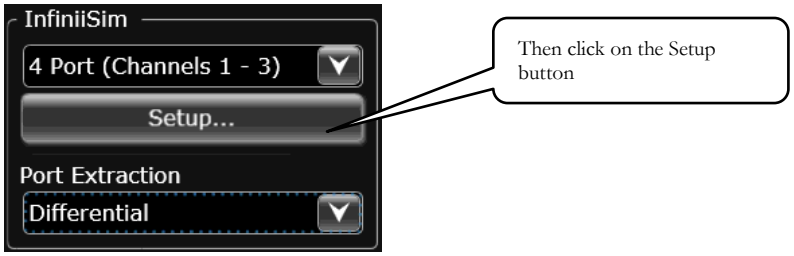


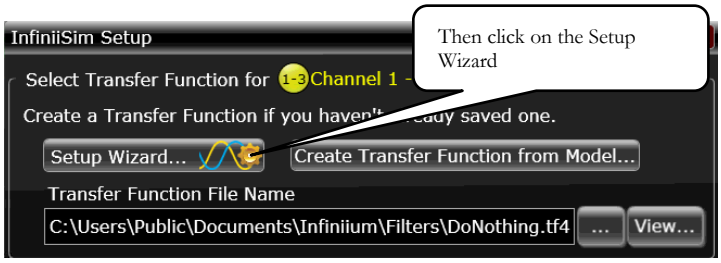
2. Setup the oscilloscope to capture 2M UI of transmitter data only as described in the "Oscilloscope Setup" section of this document.

3. Adding package model losses. Since PCIe 4.0 is a die-pad to die-pad standard it is necessary to apply the root complex package model to the waveforms that you plan to capture and then process later using SigTest. To do this you need to first make sure that your oscilloscope is licensed to support the InfiniiSim Waveform Transformation Toolset (if you need to obtain a license please contact you Keysight representative).

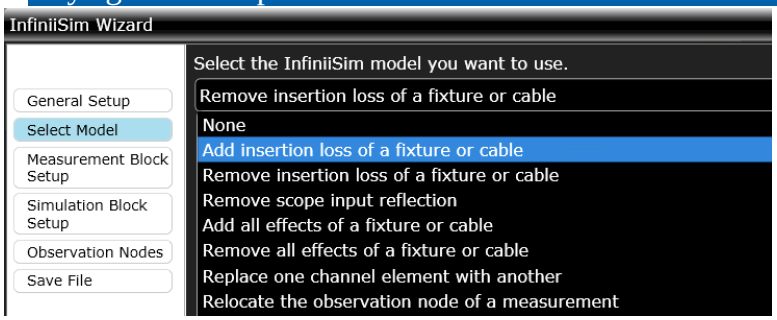
   a) This procedure assumes you are setup to use hardware differential channels 1-3. Select the drop-down menu **Setup -> Channel 1…**

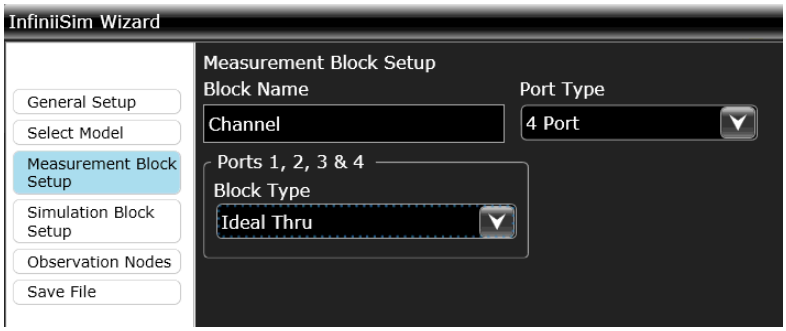
   b) In the InfiniiSim dialog box select **4 Port (Channels 1-3)**. Then click **Setup**. Then click the **Setup Wizard**.



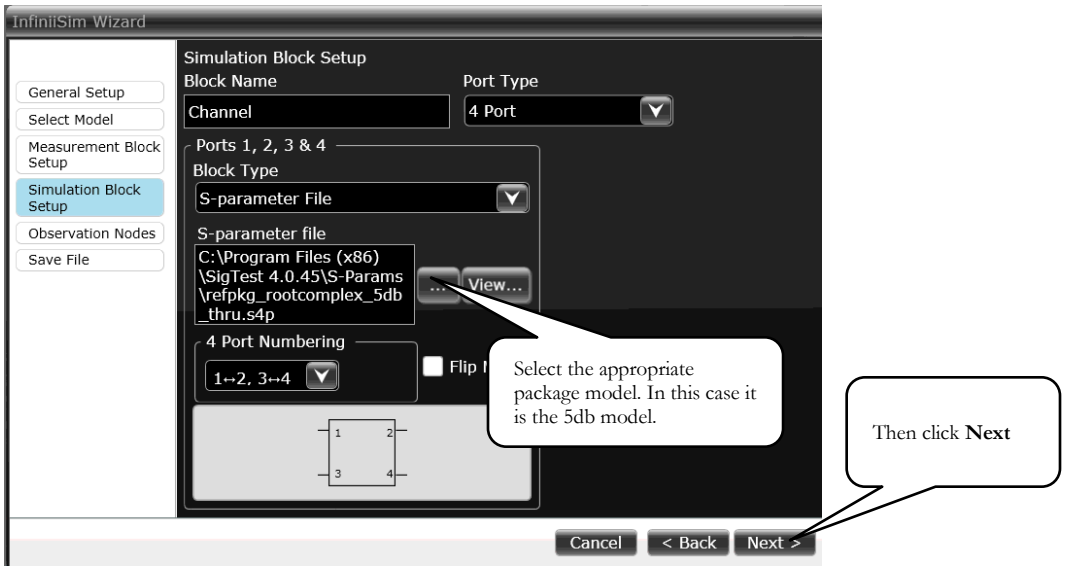


   c) Follow along with the steps that the Setup Wizard takes you through, clicking **Next** as needed until you get to the page where it asks, **Select the InfiniiSim model you want to use**.

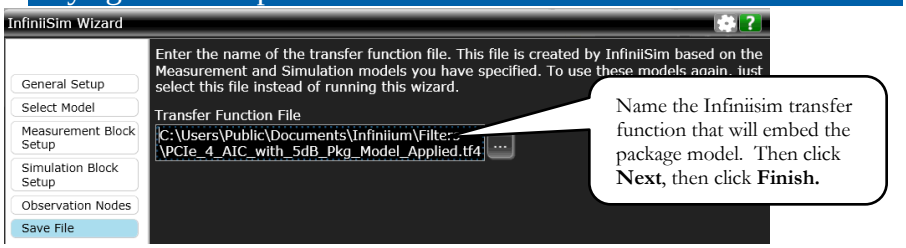




d) Once you get to the **Simulation Block Setup** in the wizard, you need to specify the PCI-SIG's root complex reference package model that is included with the SigTest 4.0.45 distribution (or later) in the S-Params directory of the SigTest installation folder. The file you want is called: *refpkg_rootcomplex_5db_thru.s4p*.



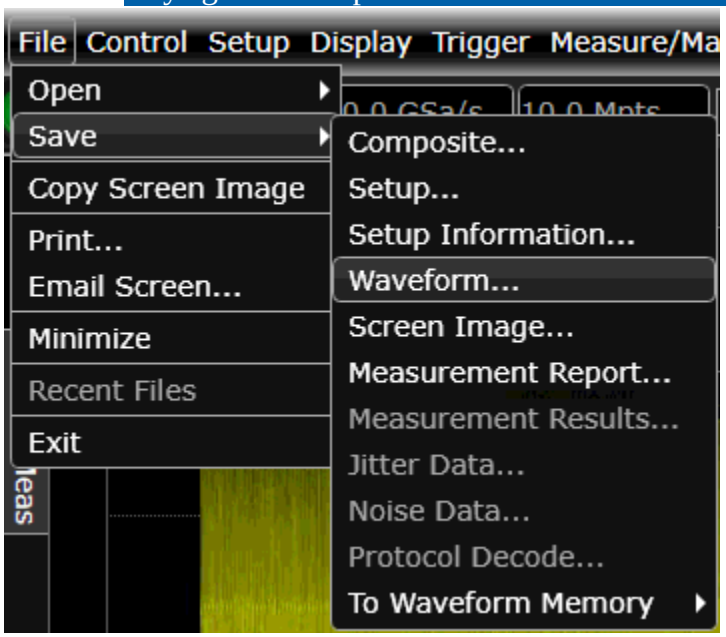
e) Now you must name the transfer function you will use to apply the reference package model. You only have to do this once assuming you do not change the measurement setup environment (channel assignments) so in the future you can bypass the InfiniiSim setup and just recall this package model once the setup has been completed.



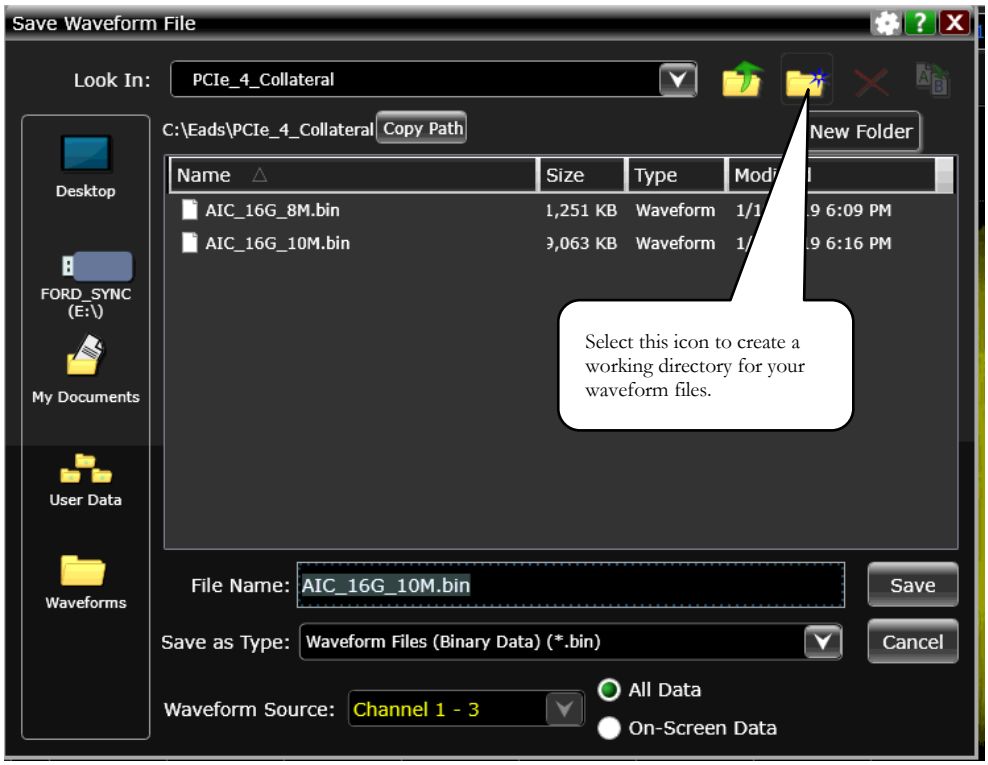
f) Once the transfer function is computed by the oscilloscope software, close out of the dialogs and return to the main Infiniium oscilloscope home screen. On this screen you will now see the DUT's waveform with the 5dB package model applied.

4. Press the Compliance Mode Toggle Button on the CBB4 until you arrive at Gen4 P0. It may help to first rest the DUT and count off the proper sequence of button pushes until you cycle through the 2.5G, 5G and 8GT/s compliance signals. The PCI-SIG's compliance program requires that you pass the PCIe 4.0 CEM signal quality test with one of the presets (P0-P11). You can choose to test any preset you prefer; however, in preliminary testing we have found that Preset P5 usually gives passing results with most devices tested thus far. You may test other presets but one must pass to be in compliance.

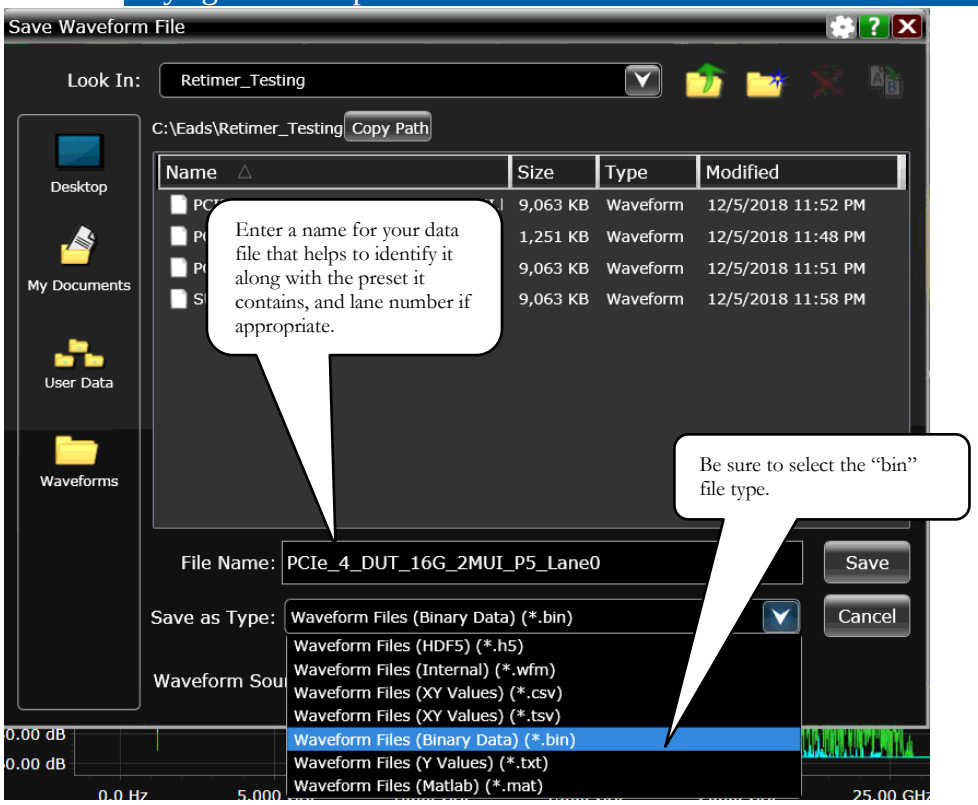
Waveform Capture. Once you have selected the proper 16GT/s preset that you want to test, select **File -> Save -> Waveform** from the drop-down menu on the oscilloscope.



Then select the new folder icon in order to create a new folder in your directory of choice.



When you have selected your directory, then pick an appropriate name for your data file and save that file as a "**Type Waveform Files (Binary Data (*.bin)**"

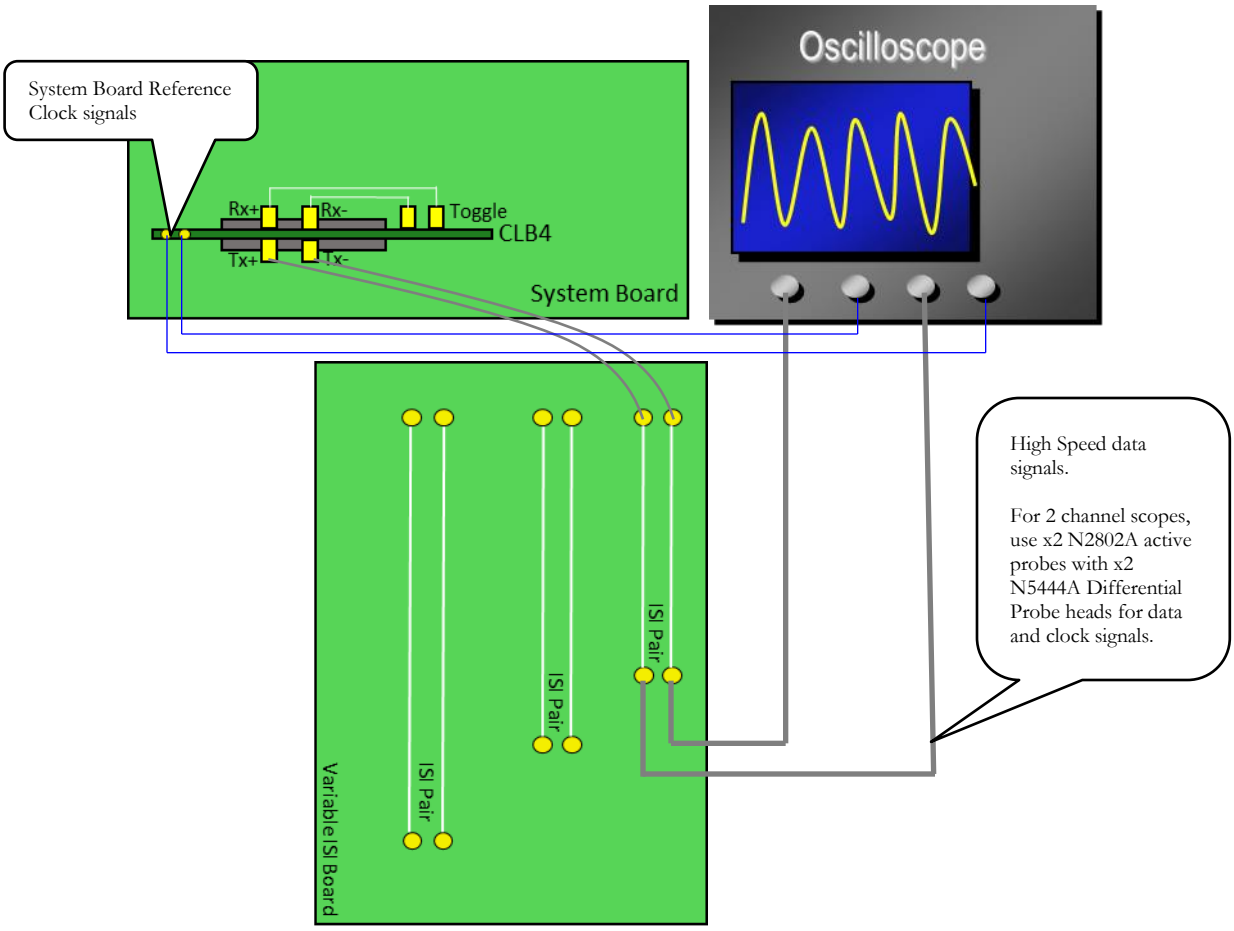


5. Test all TX lanes that the device support, saving waveform files with the appropriate preset as needed. To do this change your connection to the CBB4 that you want to test next, being sure to continue to maintain 50-ohm terminations on all lanes not being tested.

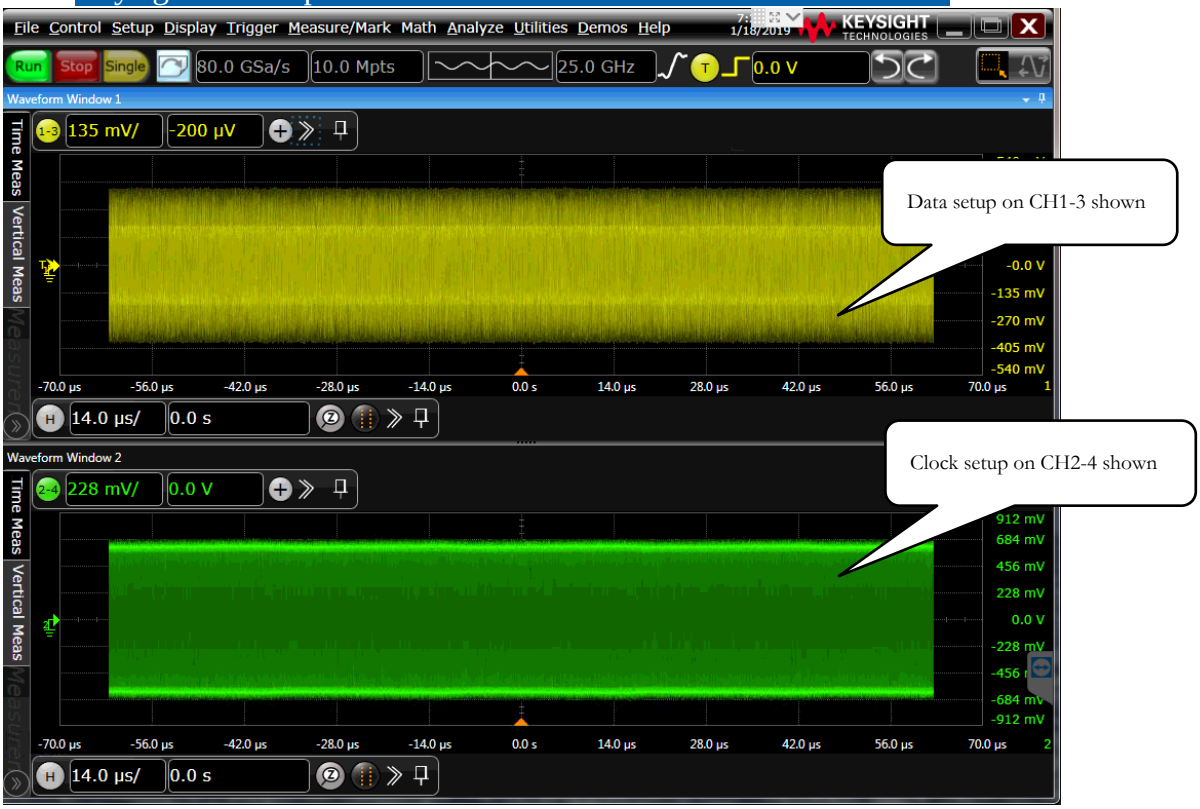
[PHY 2.7] System Board Transmitter Signal Quality Test for 16GT/s.

This section of the test procedure verifies that the signaling of the System Board device meets the eye diagram and other requirements. Lanes that are not being tested should be terminated with 50-ohm SMP terminators.

1. Configure the measurement connection setup as indicated below. Note that this is an end-of-channel test and as such requires that you emulate the maximum allowable channel loss as per the PCIe 4.0 CEM connection. The particular ISI pair that you use for this setup is determined by a number of factors including the loss of your cables, your particular CEM fixture, and adapters. For more detail on characterizing your fixtures and cables, please refer to the 2018 US Devcon presentation entitled, "PCIe® 4.0 Electrical Compliance Testing Deep Dive". Assuming you are using the recommended cables listed in the beginning of this document, we will assume "pair 0" has the appropriate amount of loss but you should verify this independently.



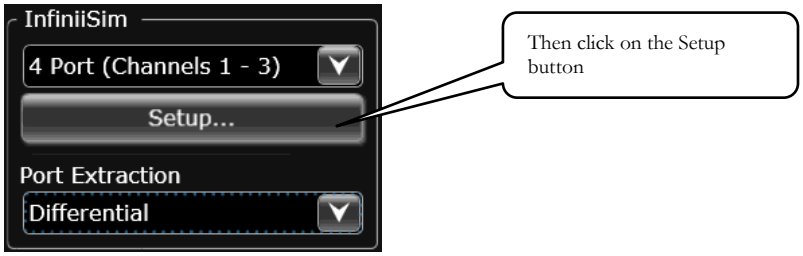
2. Setup the oscilloscope to capture 2M UI of transmitter data only as described in the "Oscilloscope Setup" section of this document. Note that in this case you will be testing the system board so setup the oscilloscope such that you are able to capture both the data signal and the clock signal at the same time as shown below.



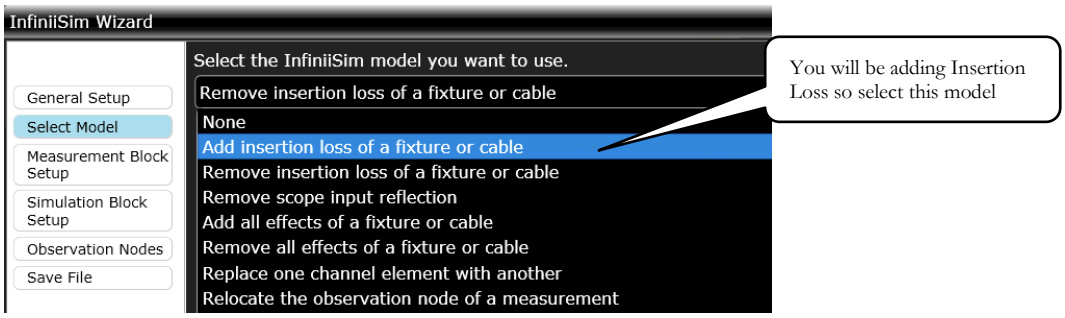
3. Adding package model losses. Since PCIe 4.0 is a die-pad to die-pad standard it is necessary to apply the end point package model to the waveforms that you plan to capture and then process later using SigTest. To do this you need to first make sure that your oscilloscope is licensed to support the InfiniiSim Waveform Transformation Toolset (if you need to obtain a license please contact you Keysight representative).

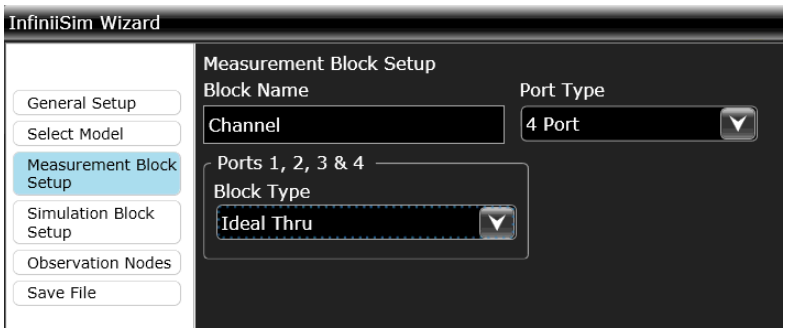
   g) This procedure assumes you are setup to use hardware differential channels 1-3. Select the drop-down menu **Setup -> Channel 1…**

   h) In the InfiniiSim dialog box select **4 Port (Channels 1-3)**. Then click **Setup**. Then click the **Setup Wizard**.

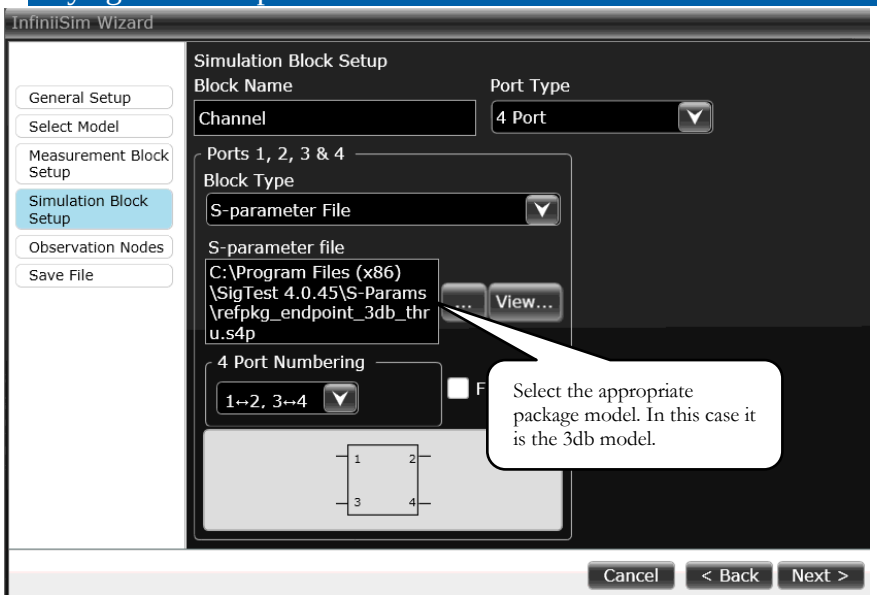


i) Follow along with the steps that the Setup Wizard takes you through, clicking **Next** as needed until you get to the page where it asks, **Select the InfiniiSim model you want to use**.

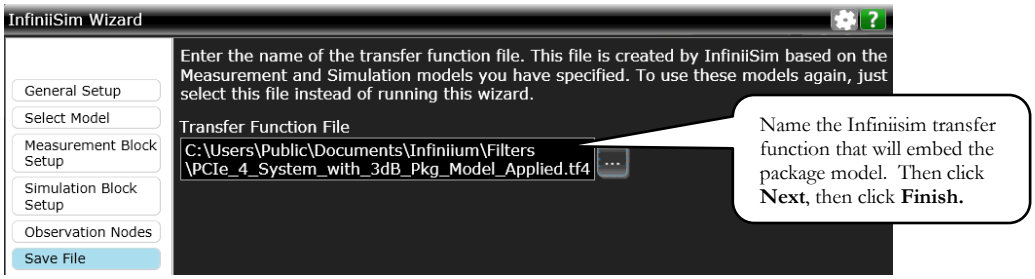




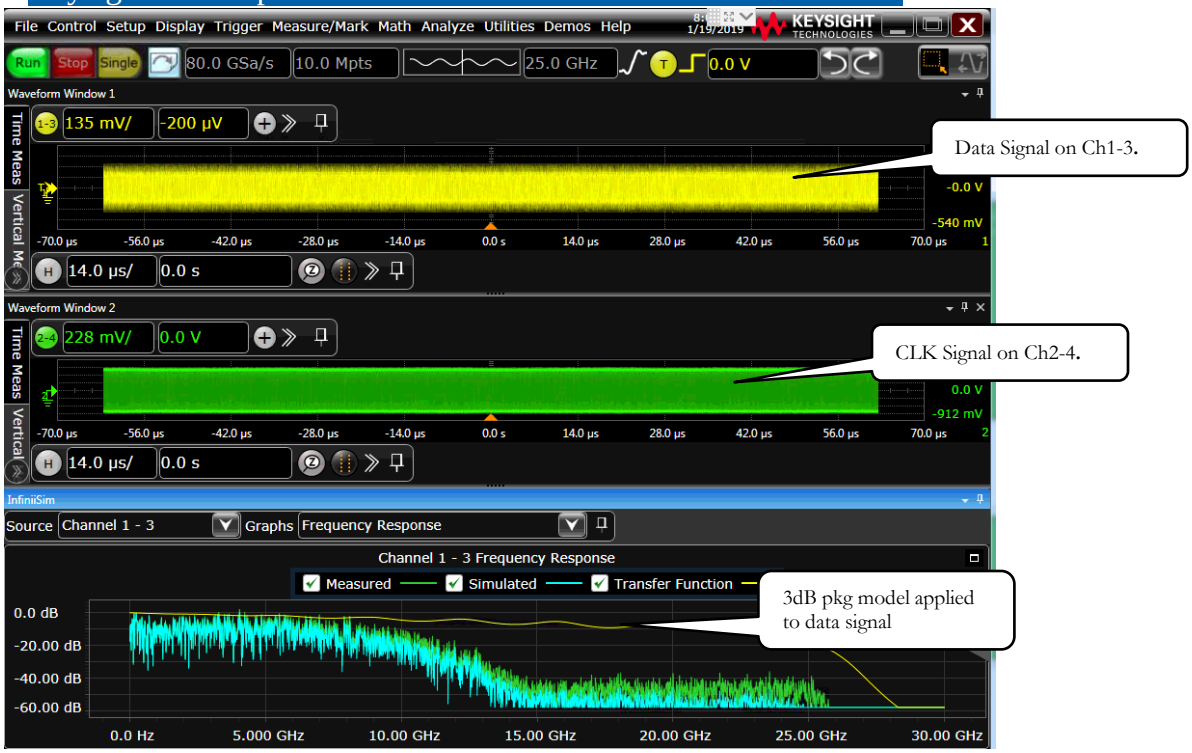
j) Once you get to the **Simulation Block Setup** in the wizard, you need to specify the PCI-SIG's endpoint reference package model that is included with the SigTest 4.0.45 distribution (or later) in the S-Params directory of the SigTest installation folder. The file you want is called: *refpkg_endpoint_3db_thru.s4p*.



k) Now you must name the transfer function you will use to apply the reference package model. You only have to do this once assuming you do not change the measurement setup environment (channel assignments) so in the future you can bypass the InfiniiSim setup and just recall this package model once the setup has been completed.

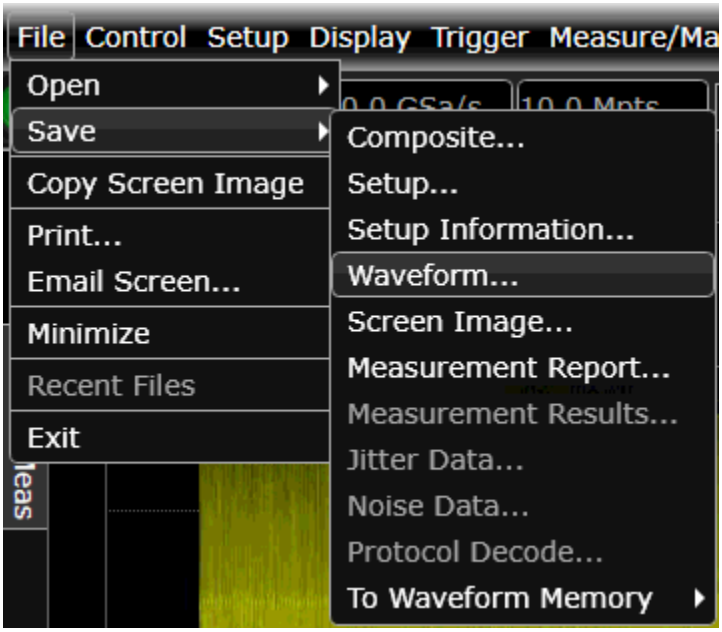


l) Once the transfer function is computed by the oscilloscope software, close out of the dialogs and return to the main Infiniium oscilloscope home screen. On this screen you will now see the DUT's waveform with the 3dB package model applied.



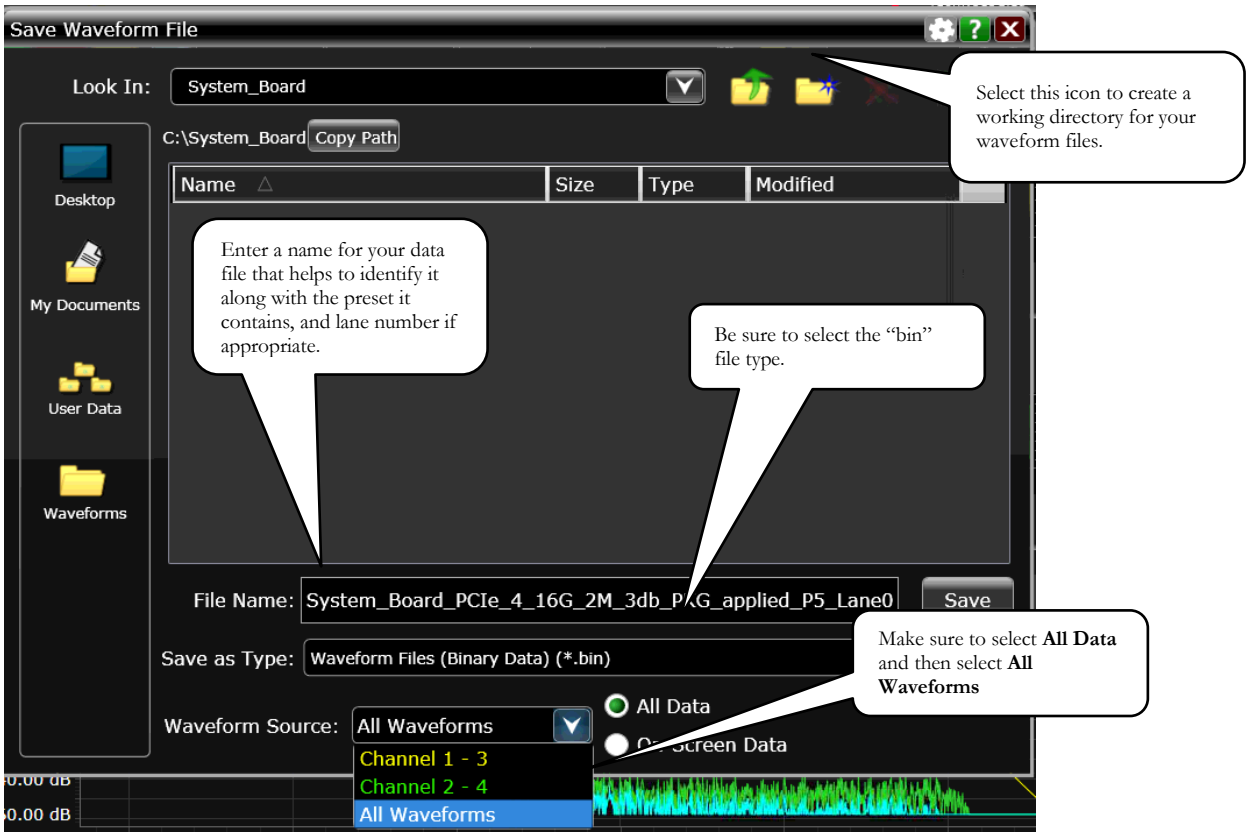
4. Press the Compliance Mode Toggle Button on the CLB4 until you arrive at Gen4 P0. It may help to first rest the DUT and count off the proper sequence of button pushes until you cycle through the 2.5G, 5G and 8GT/s compliance signals. The PCI-SIG's compliance program requires that you pass the PCIe 4.0 CEM signal quality test with one of the presets (P0-P11). You can choose to test any preset you prefer; however, in preliminary testing we have found that Preset P5 usually gives passing results with most devices tested thus far. You may test other presets but one must pass to be in compliance.

Waveform Capture. Once you have selected the proper 16GT/s preset that you want to test, select **File -> Save -> Waveform** from the drop-down menu on the oscilloscope.



Then select the new folder icon in order to create a new folder in your directory of choice. When you have selected your directory, then pick an appropriate name for your data file and save that file as a "**Type Waveform Files (Binary Data (*.bin)**"

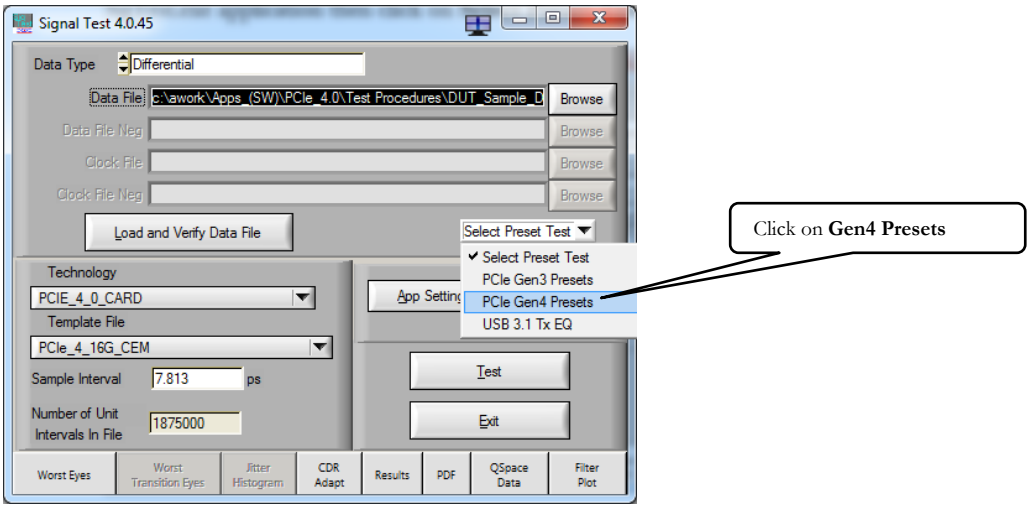
In the case of System Board waveform files be sure to also select **All Waveforms** in the Waveform Source field. This ensure that you save both the data waveform and its associated clock waveform in one file. This helps ensure that the data and clock waveforms are always together and never out of sync.



Test all TX lanes that the device support, saving waveform files with the appropriate preset as needed. To do this change your connection to the CLB4 that you want to test next, being sure to continue to maintain 50-ohm terminations on all lanes not being tested.

Post Processing Waveform Data with SigTest

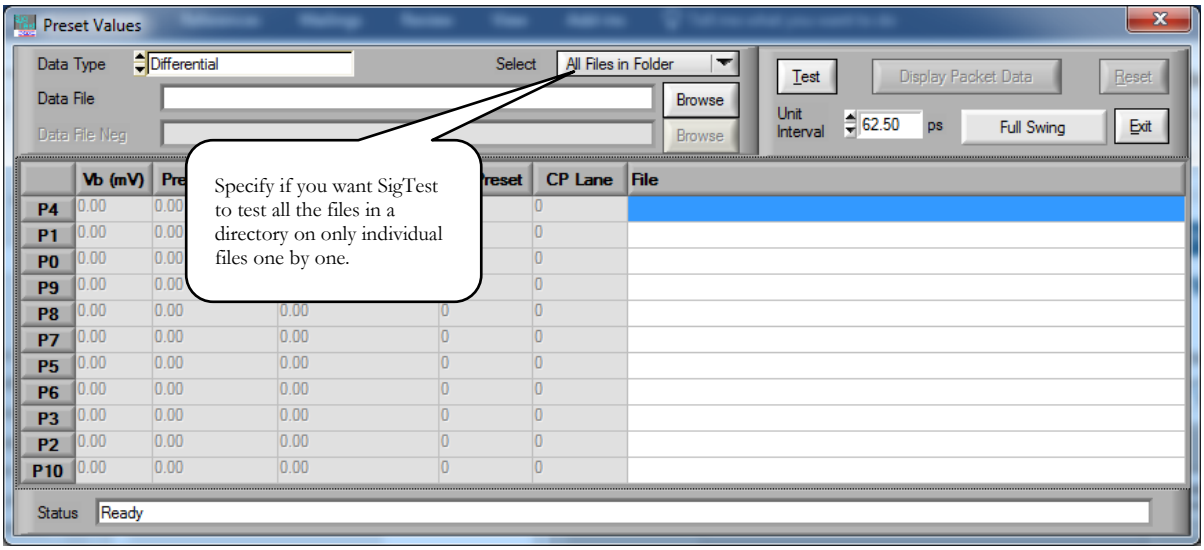
1. Preset Tests. Using Sigtest, version 4.0.45 or later, verify the presets at 16GT/s. First boot the SigTest.exe application then click on **Select Preset Test** and then click on **PCIe Gen4 Presets**.



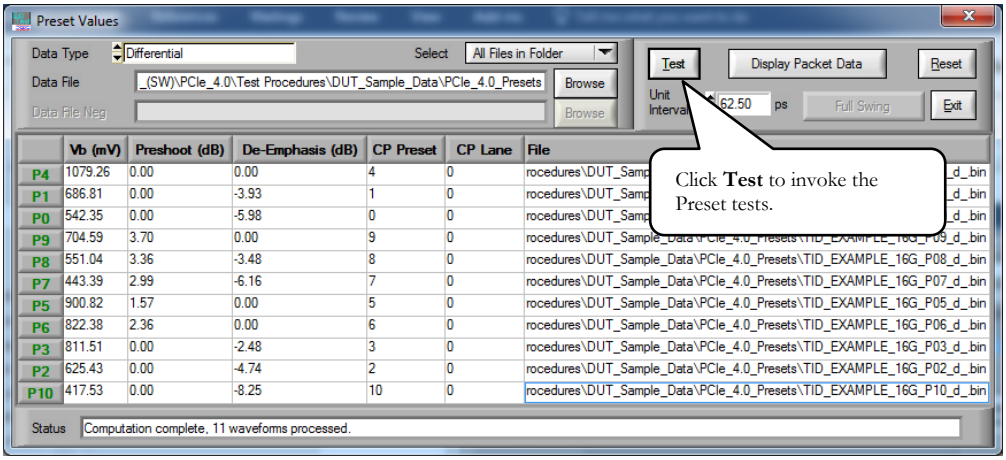
2. Next, click on **Browse** on the Preset Values Screen to select the directory where the preset waveforms have been saved.

   TIP: Using the naming convention described by the *Gen3_Preset_Instructions.docx* file included with the SigTest 4.0.45 installation, SigTest is able to automatically input and analyze all of the preset files in a given container folder. The file name should contain a substring of the form _Pnn_t_ where 'nn' is the preset number between 00 and 10 and 't' is the type of the waveform: 'd' for differential. For example, "TID1001_Ln00_P04_d_16GT.bin" indicates a differential measurement of preset 4.

   If you have not saved waveform files using this nomenclature, you can still test the presets by selecting and testing every preset waveform individually.

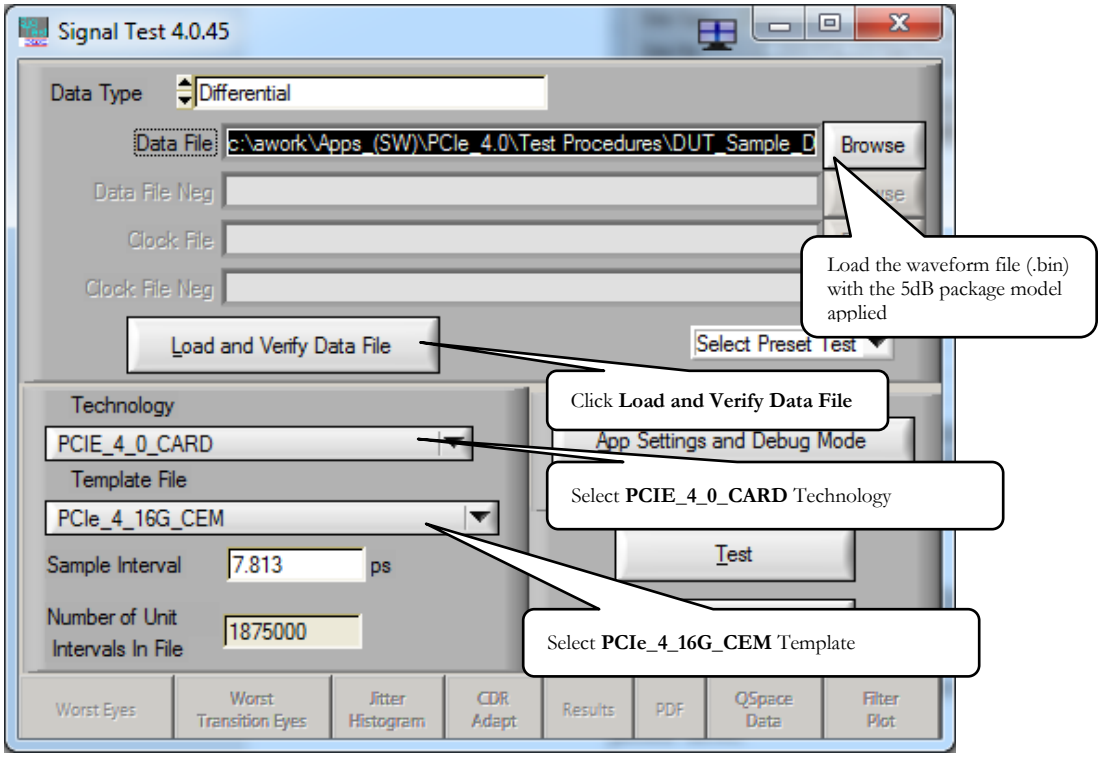


3. Once you have selected the directory where the waveform files are located, click on the **Test** button to invoke the preset test. SigTest will then load all 11 waveforms (or individual waveforms if you have chosen that mode of operation) and perform the preset test. A text file summarizing the results of the preset test will be saved to the selected waveform file directory when you press the **Exit** button.

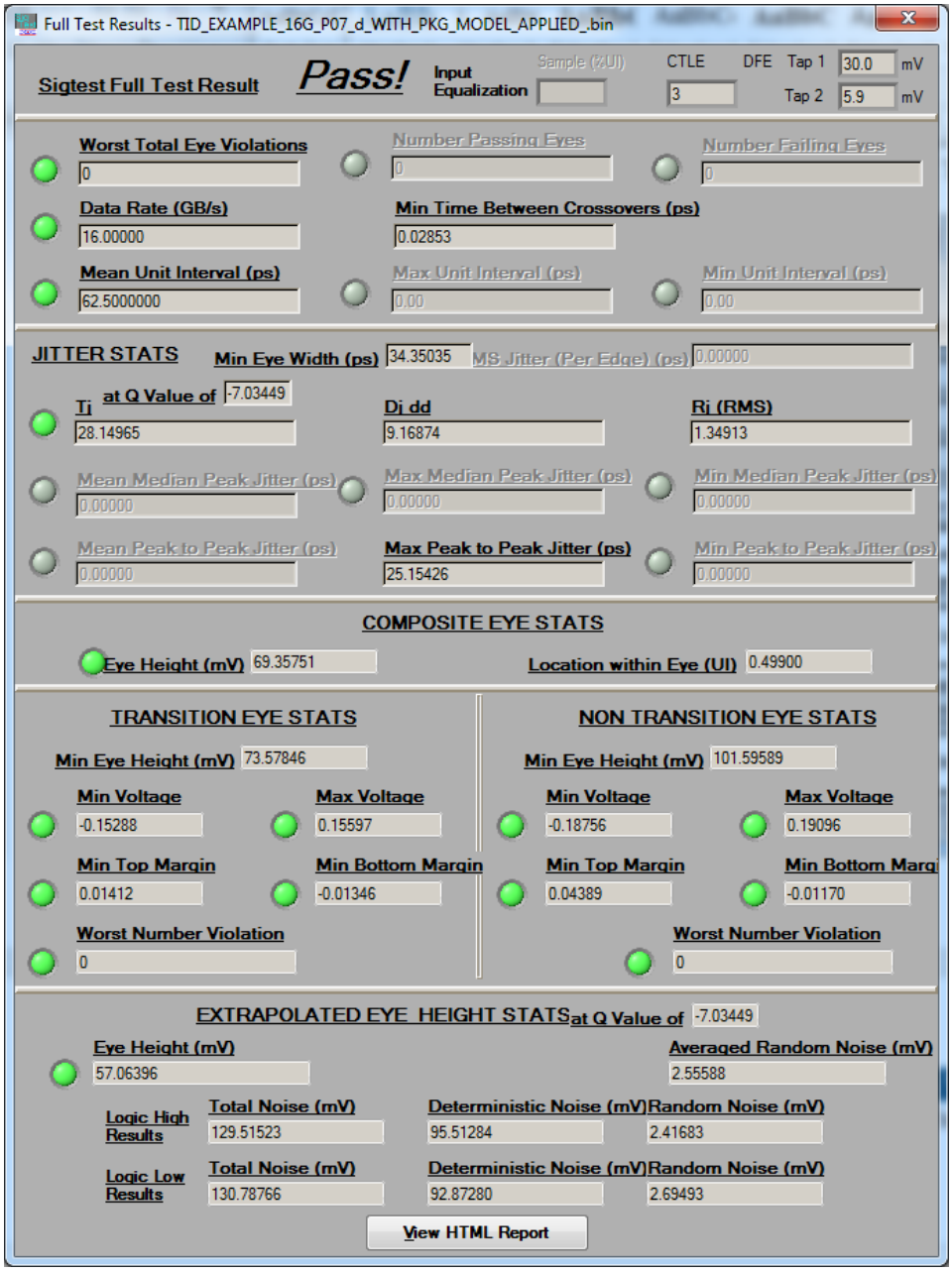


4. Signal Quality Tests: AIC. To test an add-in card (AIC) for signal quality we do two tests. The first test is the AIC signal quality data. The second test uses the clock waveform you saved while saving the preset data to perform a pulse width jitter test.

   a) To test signal quality of the add-in card you load and analyze the preset waveform that you saved which included the 5dB package model applied. The technology template you use is called ***PCIe_4_16G_CEM***. Then Click **TEST**.



b) After you click **Test**, a results screen similar to that shown below will appear after the data waveform analysis is completed.



c) You are required to pass the signal quality tests for one preset. If the preset you have chosen does not pass the signal quality test, you may choose any other preset to test. Only one preset for a given device and lane must pass.

d) Repeat the SigTest signal Quality Test for every lane you wish to test.

e) Pulse Width Jitter Test. From the main Sigtest Screen load the clock pattern or toggle pattern you saved previously. Select the ***PCIe_4_16GB_Tx_PWJ*** template and then click **Test**.

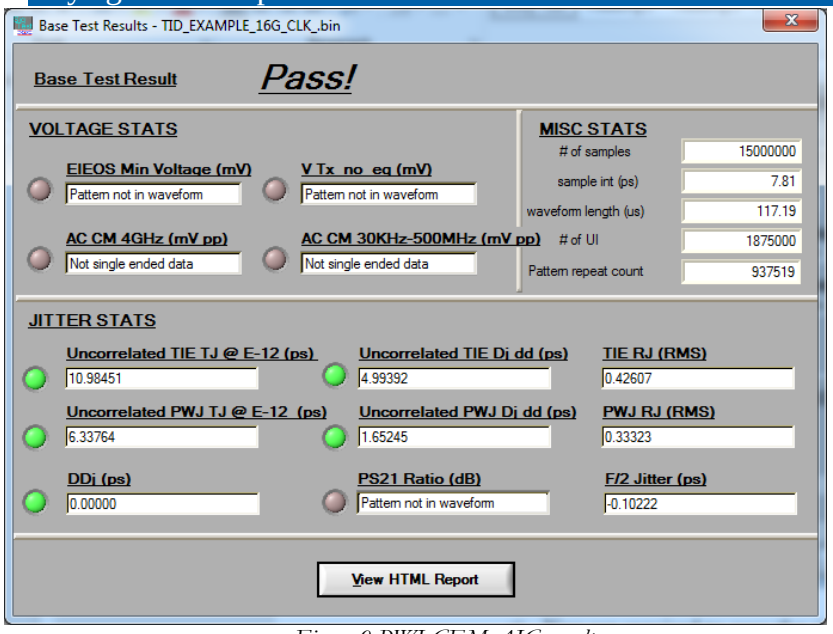
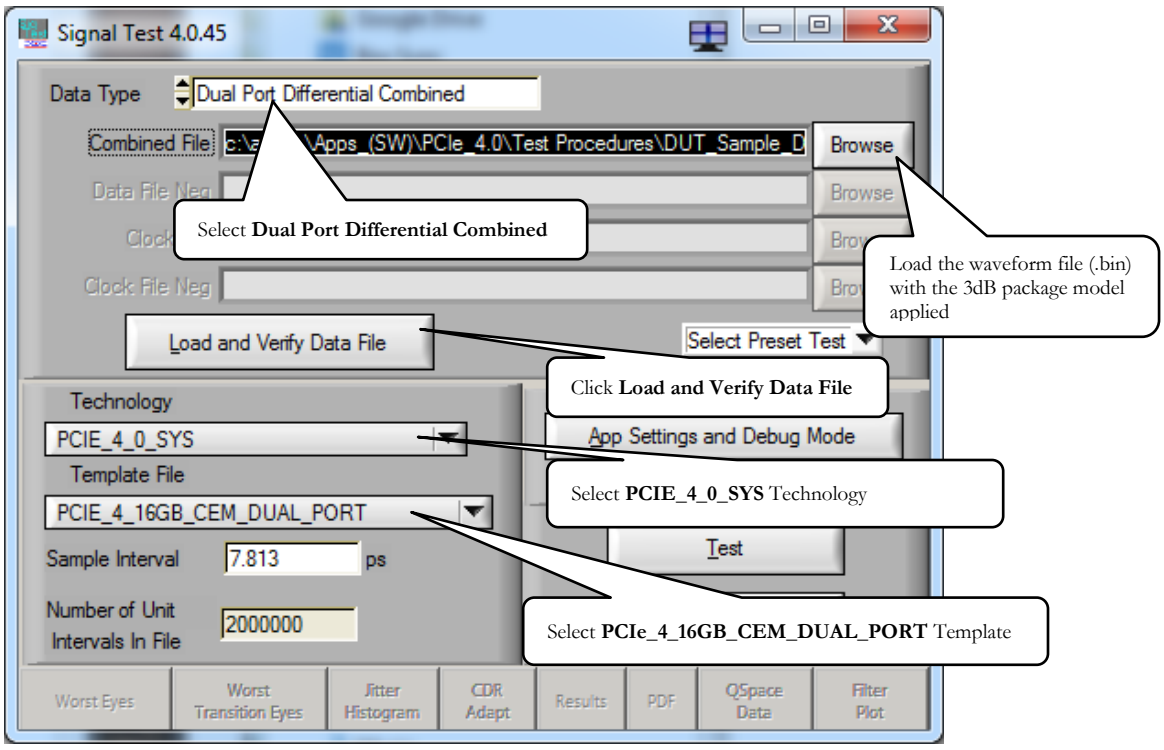


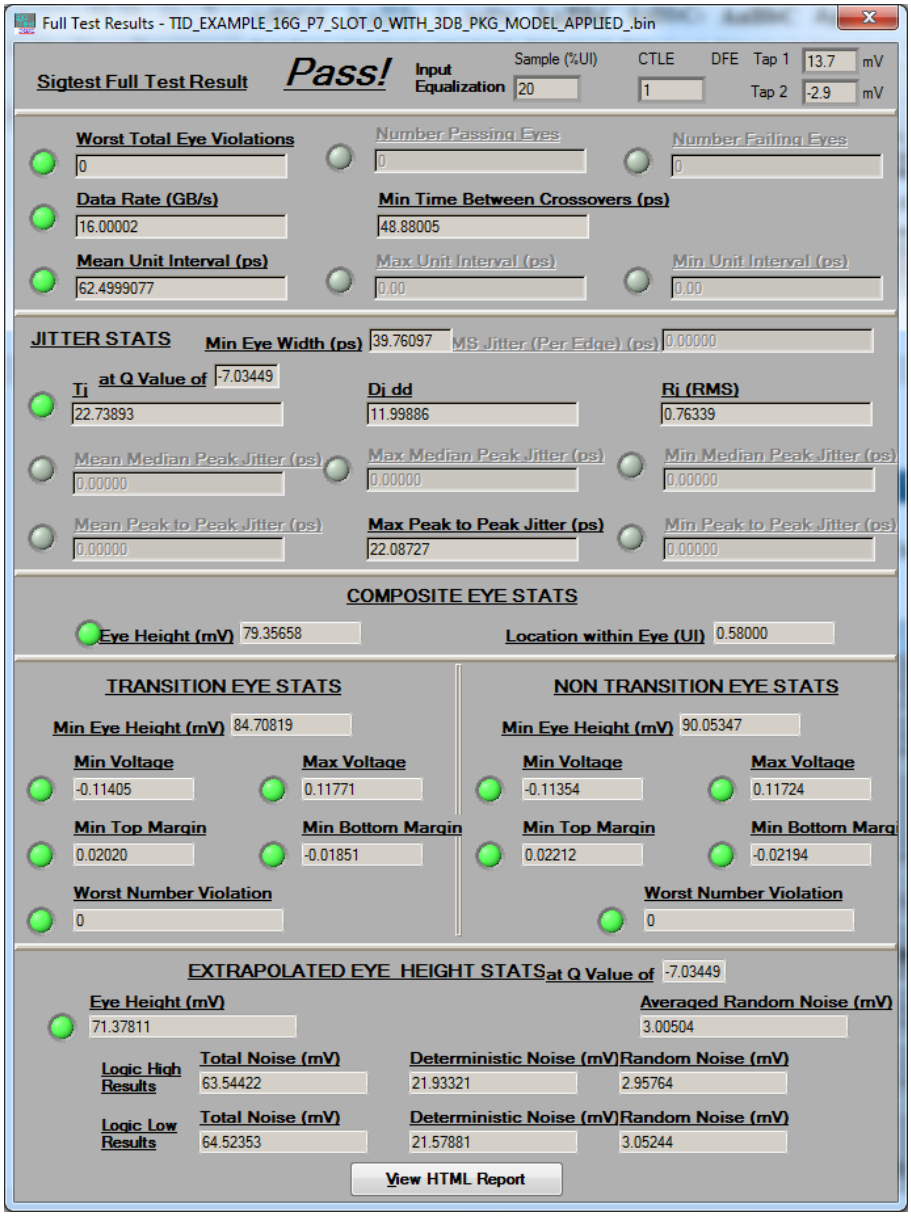
Figure 9 PWJ CEM AIC results

5. Signal Quality Tests: System Board. To test a system board for signal quality we need to load the proper waveform. In the case of system board tests, it is important to note that the data type must be changed to **Dual Port Differential Combined**.

   a) To test signal quality of the system board you load and analyze the preset waveform that you saved which included the 3dB package model applied and should also include both data and clock in the file. The technology template you use is called ***PCIe_4_16GB_CEM_DUAL_PORT***. Then Click **TEST**.



b) After you click **Test**, a results screen similar to that shown below will appear after the data waveform analysis is completed.



c) You are required to pass the signal quality tests for one preset. If they preset you have chosen does not pass the signal quality test, you may choose any other preset to test. Only one preset for a given device and lane must pass.

d) Repeat the SigTest signal Quality Tests for every lane you wish to test.