WHITE PAPER

The Fast Track to PCIe® 5.0

Doubling the Throughput of PCIe 4.0 to 32 GT/s

Data center operators need to embrace next-generation technologies to support the response times and high bandwidth requirements of 5G and IoT. With the expectation of billions of internet-connected devices and data-intensive real-time applications, 100 gigabit Ethernet (GE) speeds that are common in data centers today will not be fast enough. As a result, data center operators need to migrate their networks from 100GE to 400GE. Faster networking speeds require faster memory and faster serial bus communications.

In parallel with transceiver upgrades to 400GE, data center operators must transition to the next generation of high-speed computing interfaces. Double date rate (DDR) memory will move from DDR 4.0 to DDR 5.0, and Peripheral Component Interconnect Express (PCI Express® or PCIe®) expansion bus will move from PCIe 4.0 to PCIe 5.0.

PCIe is a high-speed, differential, serial standard for point-to-point communications at the rack-level in a data center. Data center operators prefer to assign computing tasks to servers located in the same rack to avoid inundating the data center network with unnecessary traffic. The PCIe 5.0 standard is on a fast track for development as the PCI Special Interest Group (PCI-SIG®) — the standard body that defines the PCIe specifications — plans to complete the PCIe 5.0 standard in 2019.

Three key takeaways for PCIe 5.0:

- Paves the way for 400GE in the data center
- Will double the throughput of PCIe 4.0 to 32 GT/s
- Introduces new design and test challenges

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PCIe 5.0 Will Double the Throughput of PCIe 4.0

Each new generation of the PCIe standard provides additional features and faster data transfer rates than the previous generation. PCIe 5.0 will double the throughput of PCIe 4.0. The transfer rate of PCIe 5.0 is 32 gigatransfers per second (GT/s) vs. the 16 GT/s supported by PCIe 4.0. With 64 gigabytes per second (GB/s) of unidirectional transfer bandwidth, PCIe 5.0 provides data throughput at 128 GB/s of bidirectional traffic. PCIe interconnect technology is the basis of development for many other rack-based data center technologies such as storage and graphics processing units (GPUs).

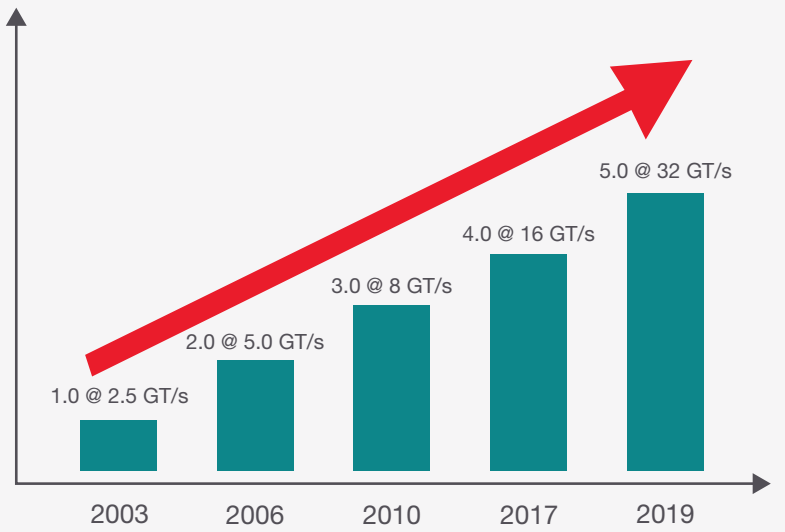

Figure 1: Evolution of the PCIe standard

If You Build It, They Will Come

Although the PCI-SIG plans to finalize the PCIe 5.0 standard in 2019, it usually takes about a year for next-generation hardware to become available in the market. The adoption of PCIe 5.0 in the data center depends on support for the standard in the servers. Nevertheless, chipset and module manufacturers have already begun working on PCIe 5.0 devices.

The overwhelming concern for designers is interoperability and backward compatibility. Designers need tools to validate the parametric and protocol aspects of their designs to ensure performance and compliance to the standard. Higher data rates increase signal integrity symptoms such as reflections and crosstalk, causing signal degradation and timing issues. A shorter clock cycle means a smaller jitter budget, so reducing jitter in PCIe 5.0 designs is far more complex than in previous generations of the standard. PCIe test is necessary at the physical layer, data link layer, and transaction layer.

PCIe 5.0 Introduces New Design and Test Challenges

It is critical for designers to gain insight into PCIe designs early in the design cycle. Using the right test solutions at each stage of development ensures the highest design quality, compliance to the PCIe standard, and interoperability with devices from other vendors. Validating PCIe performance involves characterizing the reference clock and data signals.

For Card Electromechanical (CEM) specifications, the PCI-SIG provides the Compliance Base Board (CBB), the Compliance Load Board (CLB), and SigTest software to facilitate electrical compliance testing. PCIe devices must successfully pass “Gold Suite” testing, a superset of what the PCI-SIG SigTest software tests, at a PCI-SIG workshop using the official PCI-SIG approved test fixtures. Designers using test tools that provide complete PCIe standard support ensure that their PCIe devices will pass all compliance tests before attending a workshop.

PCIe test solutions ensure:

- Highest design quality
- Compliance to the PCIe standard
- Interoperability with devices from other vendors

PCIe Design and Simulation

Designing high-speed serial data links becomes significantly more complex as data rates increase. Channel topologies become more diverse, and more parameters need to be tuned for active components. Simulating PCIe designs optimizes signal and power integrity and enables the analysis of the electromagnetic (EM) effects of components such as high-speed integrated circuit (IC) packages and printed circuit board (PCB) interconnects. Using design and simulation tools, designers can quickly and effectively evaluate end-to-end performance of all PCIe links before the first prototype, which prevents costly redesign cycles.

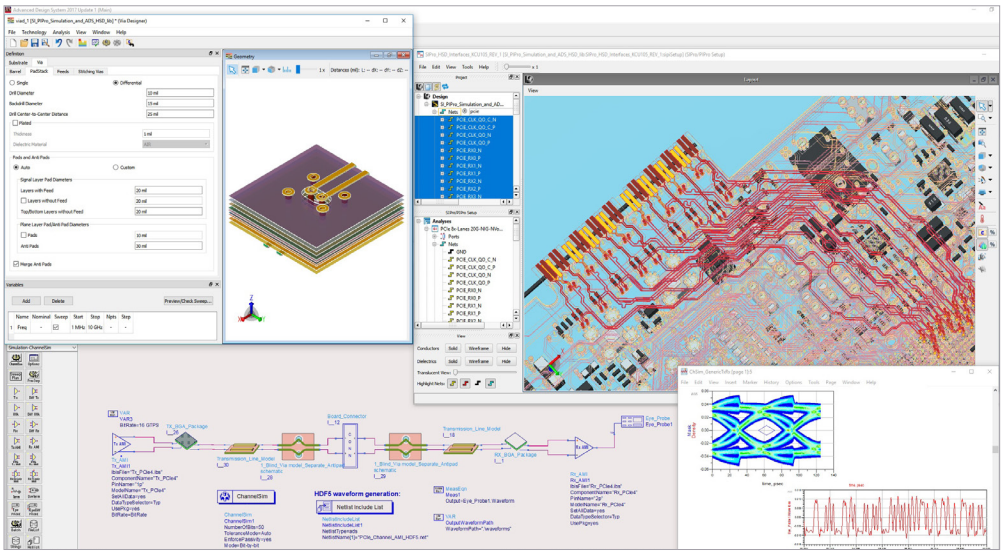

Figure 2: Keysight’s ADS high-speed digital design and simulation software

PCIe Transmitter Test

Specific types of uncorrelated jitter values are a primary concern in PCIe transmitter test. For PCIe speeds that exceed 8 GT/s, PCIe receivers utilize strong equalization. While the equalizer can compensate for data-dependent jitter, the reference receiver equalization specified by the PCIe standard does not adequately compensate for uncorrelated transmitter jitter. Using test tools that account for uncorrelated jitter ensures the performance of PCIe transmitter designs.

PCIe Receiver Test

Extracting digital content from the PCIe signal is significantly more challenging at the 32 GT/s speed of PCIe 5.0. At these high data transfer rates, PCIe receivers often receive a heavily degraded signal due to the channel's high-frequency loss characteristics, resulting in unacceptable bit error ratios (BERs). It is essential to design and validate a robust receiver that can tolerate these distorted signals, utilizing equalization techniques that restore the quality of the transmitted signal. The fact that PCIe 5.0 supports up to 16 lanes further complicates receiver design and debug. A robust PCIe receiver test solution that enables test automation can reduce test time from days to hours.

PCIe Interconnect Test

The channel is one of the most critical elements of the PCIe system. There are many sources of distortion in the channel that can degrade signal quality from a PCIe transmitter to the PCIe receiver — crosstalk, jitter, and intersymbol interference (ISI) are a few examples. Loss characteristics must be measured across the channel to ensure they are within limits defined by the PCIe specification for a given data rate. Scattering parameters (S-parameters) characterize high-frequency circuits such as the channel in a PCIe system. Quickly validating the parametric aspects of PCIe designs to ensure they are within the performance requirements defined by the PCIe specification is an essential part of the test process.

PCIe Protocol Test

Protocol validation occurs at the physical layer, data link layer, and transaction layer. In addition to the mandatory protocol compliance tests, the PCI-SIG recommends more than a hundred additional tests to characterize PCIe designs accurately. A key area of protocol test is link training and status state machine (LTSSM).

Link training ensures that data packets transfer reliably between link partners. Protocol analysis and exerciser tools determine whether a PCIe device can successfully communicate to its link partner. PCIe protocol test tools enable engineers to perform complex protocol tests and quickly debug any detected errors to ensure compliance of PCIe devices.

Conclusion

The PCIe standard is a core technology used to interconnect server peripherals in the data center. PCIe 5.0, the latest development of the standard, will enable the mass adoption of 400GE technologies in the data center as it provides full-duplex bandwidth of approximately 128 GB/s for a 16-lane system. Selecting the right test tools for design and simulation, characterization, and validation will ensure that PCIe devices seamlessly pass all required compliance tests and get to market faster.

For information on how Keysight's solutions can help you address your PCIe 5.0 design and test challenges, visit the following web pages:

- To accelerate the time-to-market of your gigabit digital designs, check out High-Speed Digital System Design
- To learn more about test solutions to simulate, characterize, and validate your PCIe designs, check out PCI Express (PCIe) Design and Test

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