APPLICATION NOTE

Boost the Potential of Your Type-C Designs

Solutions for USB4 link debug and optimization

Overview

This application note provides an overview of Type-C link debug and optimization using USB4 as an example. Learn how a Lane Adapter State Machine describes the behavior of the logical link layer and get step-by-step procedures for debugging and optimizing the USB link.

Type-C Technology Overview

The latest versions of USB, DisplayPort (DP), and Thunderbolt leverage the USB Type-C connector for audio/video, data, and power over a single cable. This application note will focus specifically on the USB4 logical layer link over USB Type-C.

The USB4 standard provides 20 Gbps signal rates on each of four transmit and receive lanes with the Type-C connector. USB4 also must support an x2 mode with a bonded bit rate of 40 Gbps in each direction. Even though other high-speed standards have faster data rates, USB4 works with a low-cost cable that yields an 80 Gbps link. Figure 1 shows the signaling lines on a Type-C connector for USB4.

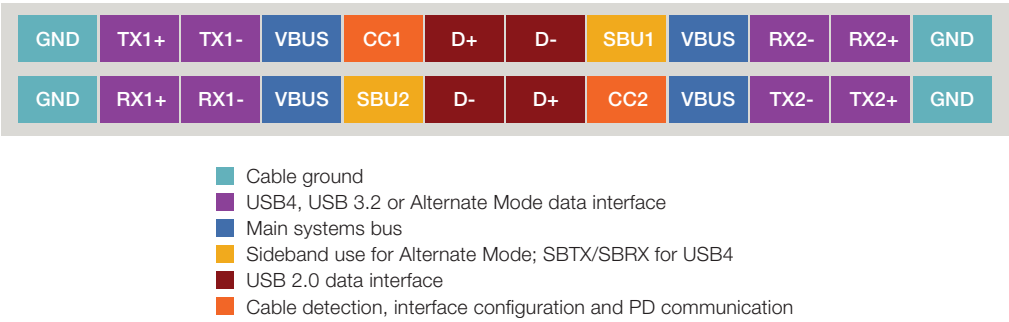


Figure 1. Type-C connector signal pins

Before we dive deeper, we need to discuss link initialization and training. Link optimization for USB 3.2 occurs directly on the transmit and receive lanes; USB 3.2 does not utilize the sideband use (SBU) lines. Link training for USB4 is different because the set-up happens via the SBU transmit (SBTX) and receive (SBRX) lines.

KEYSIGHT TECHNOLOGIES

However, there are several steps that need to happen before a USB4 link can even start. USB power delivery (USB-PD) negotiation determines that USB4 is supported, and the SBU channels communicate the link parameters for USB4. For example, the USB PD negotiation determines lanes, the re-timer type, and more prior to lane initialization and link equalization.

Solution Components for Type-C Live Link Analysis

Now that we understand a few of the various signals, we need to determine the different solutions that will access, capture, and analyze the signals. Table 1 and Figure 1 illustrate the solution components.

Keysight Solution	Description
N7019A USB Type-C Active Link Fixture	Use this fixture to access all Type-C signals in a live link (VBUS, CC for USB-PD, SBTX/SBRX, and TX/RX) for debug, decode, and analysis
D9010USBP Protocol Trigger & Decode Software	This software package provides the ability to trigger and decode on all speeds of USB signals, including USB4
D9040USBC USB4 Tx Test Software	USB4 Tx software to automatically configures the oscilloscope for each test to enable so you can characterize your designs fastquickly and easy design characterizationily.
MXR-Series Real-Time Oscilloscope	Real-time protocol triggering to captures events of interest on the CC and SBTX/SBRX lines.
UXR-Series Real-Time Oscilloscope	Captures high-speed 20 Gbps signaling for analysis and decoding at a (minimum 25 GHz bandwidth)

Table 1. An overview of the solution components

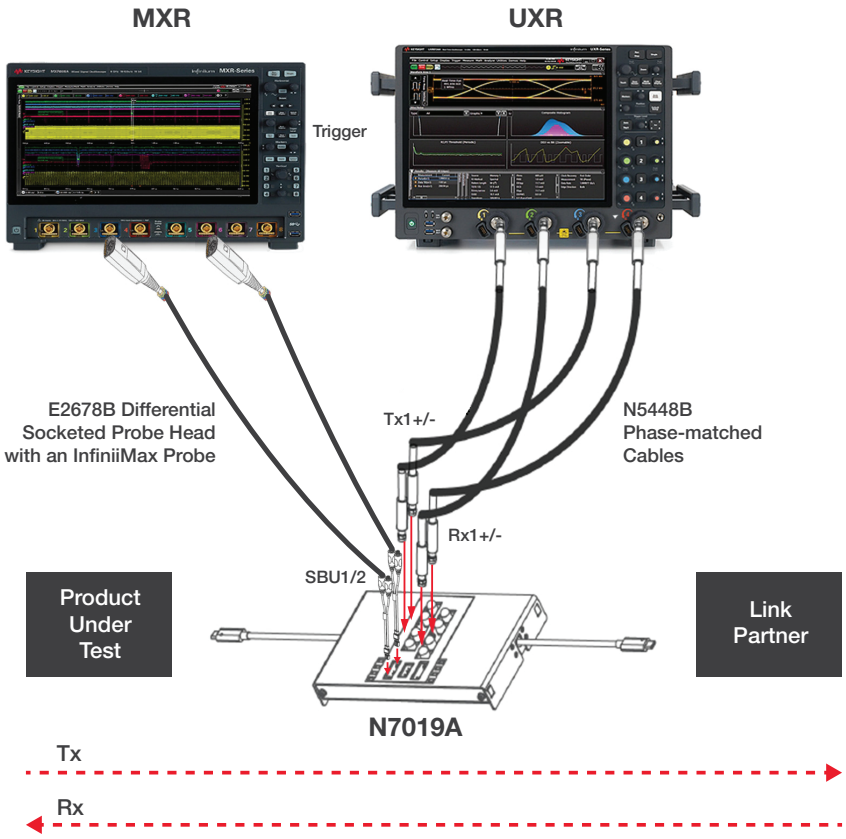


Figure 2. Test setup for USB4 Type-C link analysis

Specifications like a 20 Gbps signal rate and the need to bond to an aggregate 40 Gbps make the USB Link fairly complex. The setup requires a step-by-step plan in order for USB4 to reach its full potential.

States and Behavior of the USB4 Logical Link Layer

The Lane Adapter State Machine in Figure 3 describes the behavior of the logical link layer during the linkup sequence. The sequence includes the following steps:

- Link partners connect initially during CLd state entry (lane initialization)
- Transition to training sub-state from CLd state (transmitter and receiver lanes are on)
- Transmitter Feed Forward Equalization (TxFFE) negotiation during Training.LOCK1 sub-state
- Transition from two single-lane links to a dual-lane link via land bonding
- Link partners disconnect

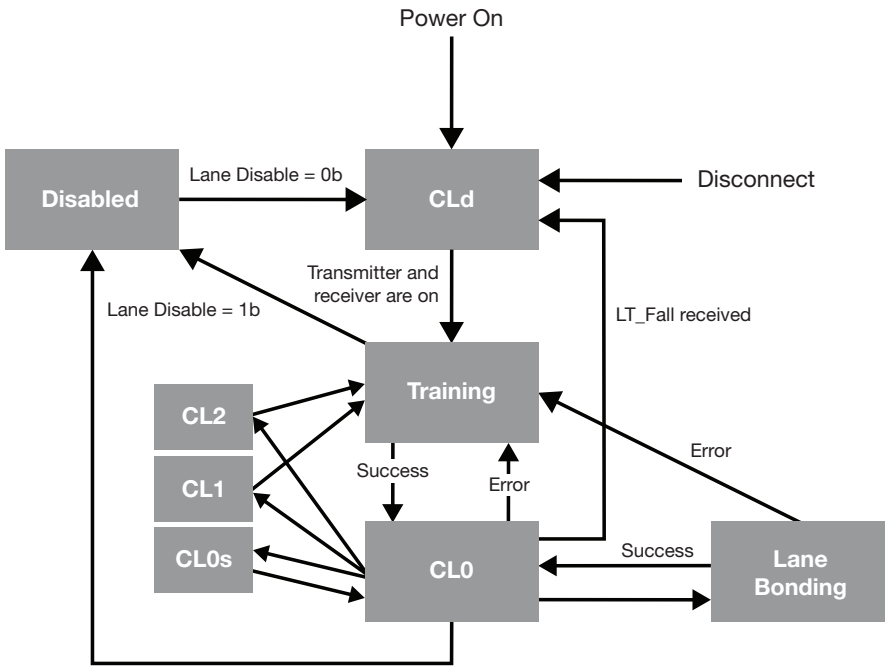


Figure 3. USB4 Lane Adapter State Machine

CLd State Entry

During initial power-on, a USB4 device under test (DUT) enters the CLd state. Figure 4 shows the D9010USBP software decoding the SBTX/SBRX sideband channel and "Read Link Config AT" packet which shows the DUT in the CLd state. An oscilloscope can confirm that the Tx and Rx lanes are inactive in this state (Figure 5).

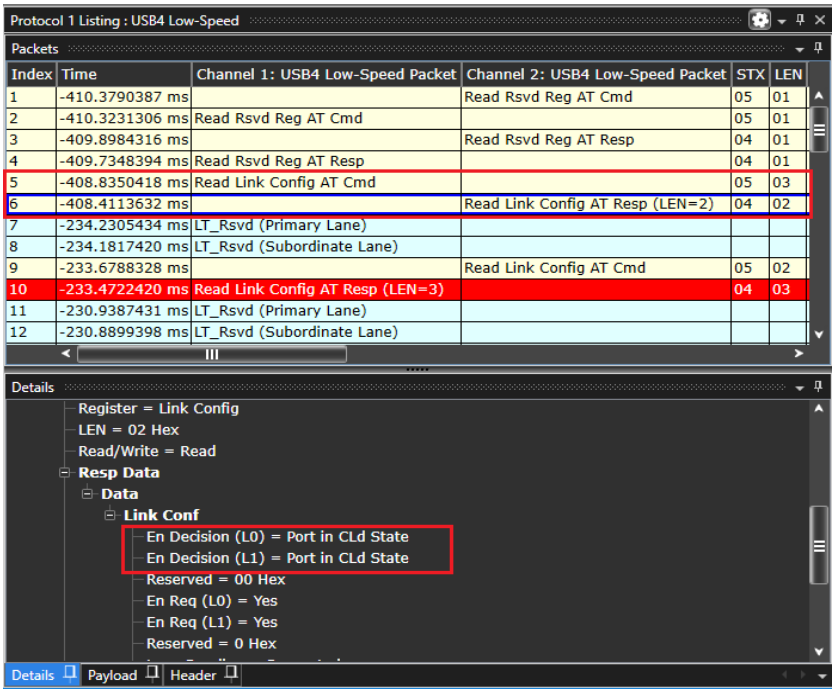


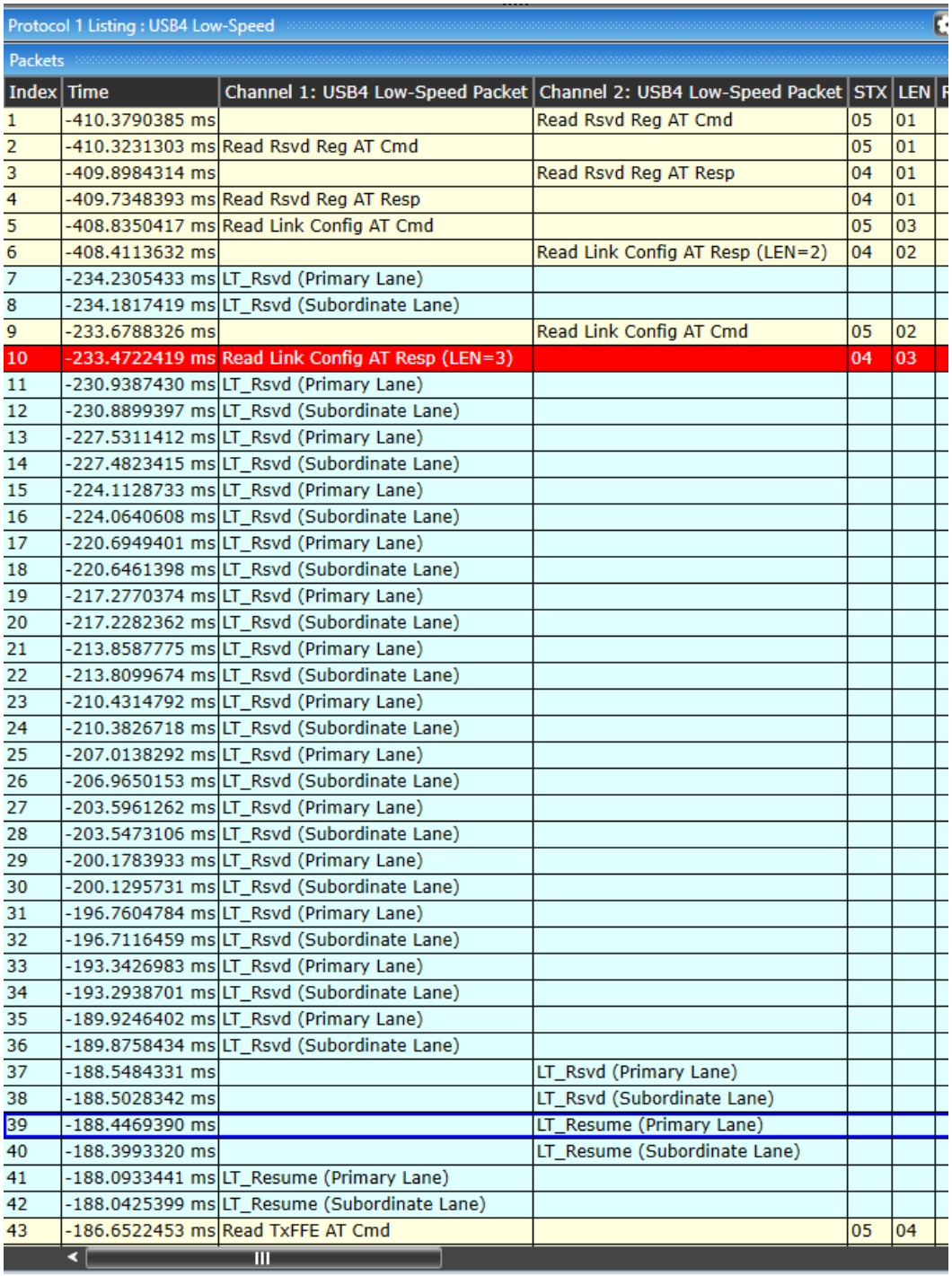
Figure 4. D9010USBP CLd state decode

Figure 5. UXR oscilloscope displays inactive Tx and Rx lines

Transition to Training.LOCK1 Sub-State from CLd State

Primary Lane

A lane adapter transitions to the Training.LOCK1 sub-state where symbols synchronize, and parameters transfer between the ends of the lane. You can see this on the SBTX/SBRX lines by triggering on the “LT_Resume (Primary Lane)” packet (Figure 6). The Tx and Rx lanes remain active during this transition. Using the oscilloscope, you can see the back-to-back symbol lock ordered set (SLOS1) in Figure 7. The SLOS1 is a pseudo-random binary sequence (PRBS11) pattern with a high number of transitions which provide more edges to facilitate clock recover and enable bit lock.

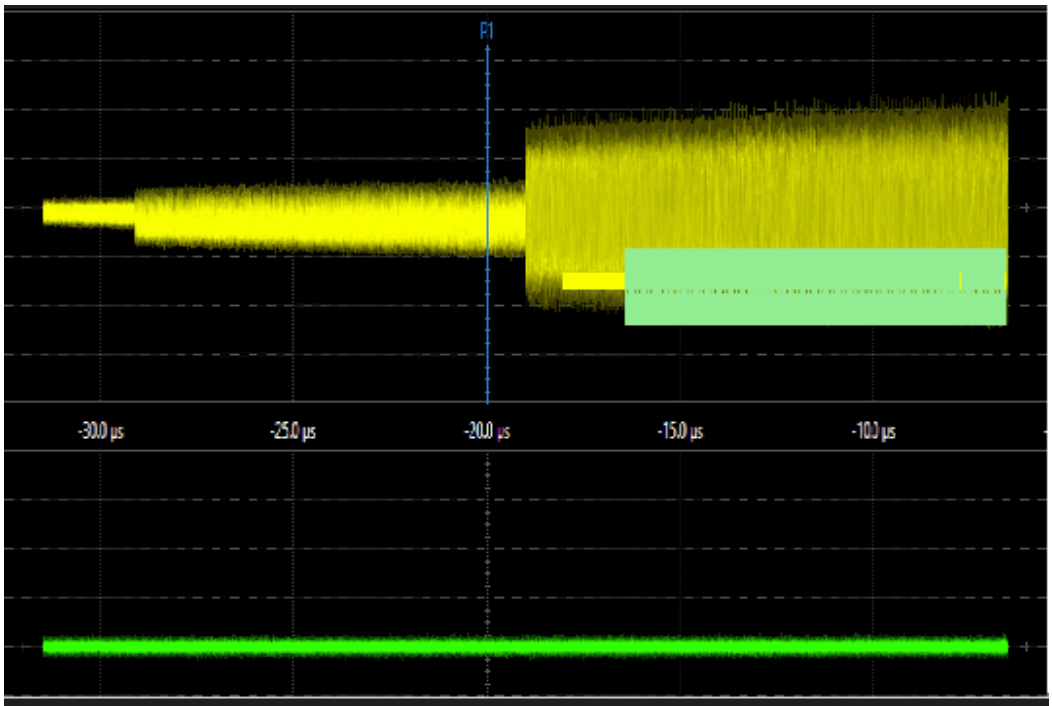


Protocol 1 Listing : USB4 Low-Speed

Packets

Index	Time	Channel 1: USB4 Low-Speed Packet	Channel 2: USB4 Low-Speed Packet	STX	LEN
1	-410.3790385 ms		Read Rsvd Reg AT Cmd	05	01
2	-410.3231303 ms	Read Rsvd Reg AT Cmd		05	01
3	-409.8984314 ms		Read Rsvd Reg AT Resp	04	01
4	-409.7348393 ms	Read Rsvd Reg AT Resp		04	01
5	-408.8350417 ms	Read Link Config AT Cmd		05	03
6	-408.4113632 ms		Read Link Config AT Resp (LEN=2)	04	02
7	-234.2305433 ms	LT_Rsvd (Primary Lane)			
8	-234.1817419 ms	LT_Rsvd (Subordinate Lane)			
9	-233.6788326 ms		Read Link Config AT Cmd	05	02
10	-233.4722419 ms	Read Link Config AT Resp (LEN=3)		04	03
11	-230.9387430 ms	LT_Rsvd (Primary Lane)			
12	-230.8899397 ms	LT_Rsvd (Subordinate Lane)			
13	-227.5311412 ms	LT_Rsvd (Primary Lane)			
14	-227.4823415 ms	LT_Rsvd (Subordinate Lane)			
15	-224.1128733 ms	LT_Rsvd (Primary Lane)			
16	-224.0640608 ms	LT_Rsvd (Subordinate Lane)			
17	-220.6949401 ms	LT_Rsvd (Primary Lane)			
18	-220.6461398 ms	LT_Rsvd (Subordinate Lane)			
19	-217.2770374 ms	LT_Rsvd (Primary Lane)			
20	-217.2282362 ms	LT_Rsvd (Subordinate Lane)			
21	-213.8587775 ms	LT_Rsvd (Primary Lane)			
22	-213.8099674 ms	LT_Rsvd (Subordinate Lane)			
23	-210.4314792 ms	LT_Rsvd (Primary Lane)			
24	-210.3826718 ms	LT_Rsvd (Subordinate Lane)			
25	-207.0138292 ms	LT_Rsvd (Primary Lane)			
26	-206.9650153 ms	LT_Rsvd (Subordinate Lane)			
27	-203.5961262 ms	LT_Rsvd (Primary Lane)			
28	-203.5473106 ms	LT_Rsvd (Subordinate Lane)			
29	-200.1783933 ms	LT_Rsvd (Primary Lane)			
30	-200.1295731 ms	LT_Rsvd (Subordinate Lane)			
31	-196.7604784 ms	LT_Rsvd (Primary Lane)			
32	-196.7116459 ms	LT_Rsvd (Subordinate Lane)			
33	-193.3426983 ms	LT_Rsvd (Primary Lane)			
34	-193.2938701 ms	LT_Rsvd (Subordinate Lane)			
35	-189.9246402 ms	LT_Rsvd (Primary Lane)			
36	-189.8758434 ms	LT_Rsvd (Subordinate Lane)			
37	-188.5484331 ms		LT_Rsvd (Primary Lane)		
38	-188.5028342 ms		LT_Rsvd (Subordinate Lane)		
39	-188.4469390 ms		LT_Resume (Primary Lane)		
40	-188.3993320 ms		LT_Resume (Subordinate Lane)		
41	-188.0933441 ms	LT_Resume (Primary Lane)			
42	-188.0425399 ms	LT_Resume (Subordinate Lane)			
43	-186.6522453 ms	Read TxFFE AT Cmd		05	04

Figure 6. D9010USBP showing LT_Resume trigger



Protocol 1 Listing : USB 4.0 Gen 2-3

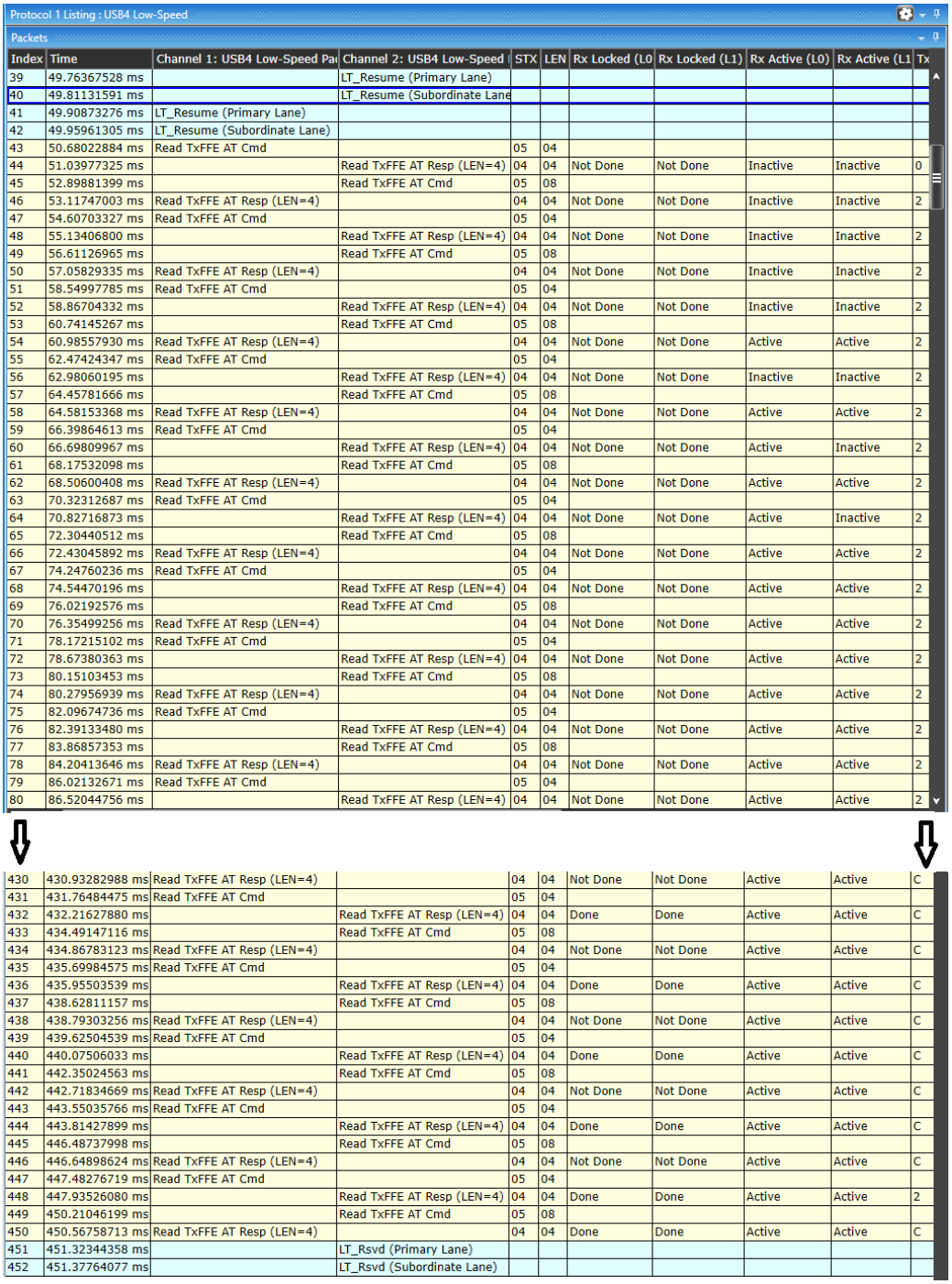
Packets

Index	Time	FEC	Channel 1 - 3: USB4 Packet	Channel 2 - 4: USB4 Packet
1	-16.37885448 µs		SLOS1 (Gen2,3)	
2	-16.27631713 µs		SLOS1 (Gen2,3)	
3	-16.17377628 µs		SLOS1 (Gen2,3)	
4	-16.07123527 µs		SLOS1 (Gen2,3)	
5	-15.96869956 µs		SLOS1 (Gen2,3)	
6	-15.86617079 µs		SLOS1 (Gen2,3)	
7	-15.76364681 µs		SLOS1 (Gen2,3)	
8	-15.66112473 µs		SLOS1 (Gen2,3)	
9	-15.55860389 µs		SLOS1 (Gen2,3)	
10	-15.45608248 µs		SLOS1 (Gen2,3)	
11	-15.35356064 µs		SLOS1 (Gen2,3)	
12	-15.25104954 µs		SLOS1 (Gen2,3)	
13	-15.14854740 µs		SLOS1 (Gen2,3)	
14	-15.04604810 µs		SLOS1 (Gen2,3)	
15	-14.94354527 µs		SLOS1 (Gen2,3)	
16	-14.84105294 µs		SLOS1 (Gen2,3)	

Figure 7. UXR oscilloscope displays decode of SLOS1

Secondary/Subordinate Lane

You must run and test USB4 DUTs in x2 mode even though single lane operation is possible. However, this means creating an additional requirement for training and optimizing a secondary lane. Figure 8 shows a trigger on LT_Resume for a subordinate lane. It is important to note that lane common mode voltage is not maintained (Figure 9).

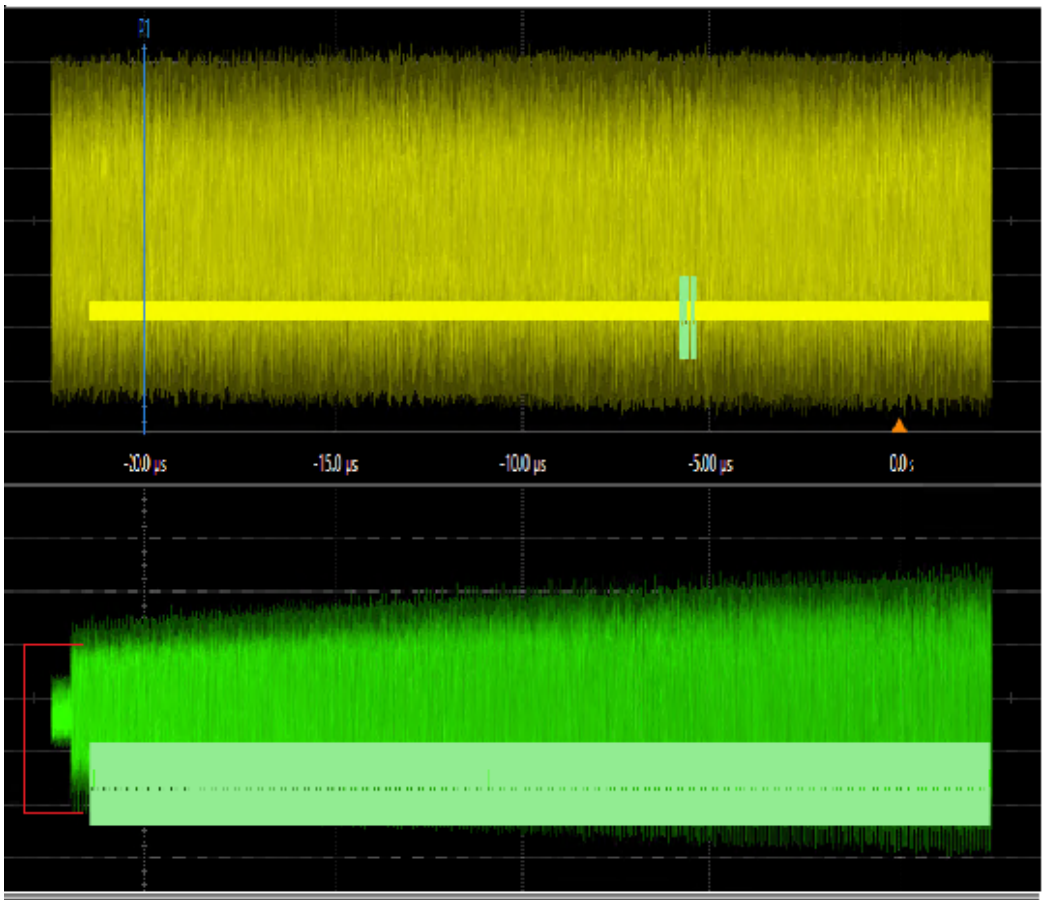


Protocol 1 Listing : USB4 Low-Speed

Packets

Index	Time	Channel 1: USB4 Low-Speed Pa	Channel 2: USB4 Low-Speed	STX	LEN	Rx Locked (L0	Rx Locked (L1)	Rx Active (L0)	Rx Active (L1	Tx
39	49.76367528 ms		LT_Resume (Primary Lane)							
40	49.81131591 ms		LT_Resume (Subordinate Lane							
41	49.90873276 ms	LT_Resume (Primary Lane)								
42	49.95961305 ms	LT_Resume (Subordinate Lane)								
43	50.68022884 ms	Read TxFFE AT Cmd		05	04					
44	51.03977325 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	0
45	52.89881399 ms		Read TxFFE AT Cmd	05	08					
46	53.11747003 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Inactive	Inactive	2
47	54.60703327 ms	Read TxFFE AT Cmd		05	04					
48	55.13406800 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	2
49	56.61126965 ms		Read TxFFE AT Cmd	05	08					
50	57.05829335 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Inactive	Inactive	2
51	58.54997785 ms	Read TxFFE AT Cmd		05	04					
52	58.86704332 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	2
53	60.74145267 ms		Read TxFFE AT Cmd	05	08					
54	60.98557930 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
55	62.47424347 ms	Read TxFFE AT Cmd		05	04					
56	62.98060195 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	2
57	64.45781666 ms		Read TxFFE AT Cmd	05	08					
58	64.58153368 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
59	66.39864613 ms	Read TxFFE AT Cmd		05	04					
60	66.69809967 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Inactive	2
61	68.17532098 ms		Read TxFFE AT Cmd	05	08					
62	68.50600408 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
63	70.32312687 ms	Read TxFFE AT Cmd		05	04					
64	70.82716873 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Inactive	2
65	72.30440512 ms		Read TxFFE AT Cmd	05	08					
66	72.43045892 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
67	74.24760236 ms	Read TxFFE AT Cmd		05	04					
68	74.54470196 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Active	2
69	76.02192576 ms		Read TxFFE AT Cmd	05	08					
70	76.35499256 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
71	78.17215102 ms	Read TxFFE AT Cmd		05	04					
72	78.67380363 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Active	2
73	80.15103453 ms		Read TxFFE AT Cmd	05	08					
74	80.27956939 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
75	82.09674736 ms	Read TxFFE AT Cmd		05	04					
76	82.39133480 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Active	2
77	83.86857353 ms		Read TxFFE AT Cmd	05	08					
78	84.20413646 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
79	86.02132671 ms	Read TxFFE AT Cmd		05	04					
80	86.52044756 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Active	2
430	430.93282988 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
431	431.76484475 ms	Read TxFFE AT Cmd		05	04					
432	432.21627880 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
433	434.49147116 ms		Read TxFFE AT Cmd	05	08					
434	434.86783123 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
435	435.69984575 ms	Read TxFFE AT Cmd		05	04					
436	435.95503539 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
437	438.62811157 ms		Read TxFFE AT Cmd	05	08					
438	438.79303256 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
439	439.62504539 ms	Read TxFFE AT Cmd		05	04					
440	440.07506033 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
441	442.35024563 ms		Read TxFFE AT Cmd	05	08					
442	442.71834669 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
443	443.55035766 ms	Read TxFFE AT Cmd		05	04					
444	443.81427899 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
445	446.48737998 ms		Read TxFFE AT Cmd	05	08					
446	446.64898624 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
447	447.48276719 ms	Read TxFFE AT Cmd		05	04					
448	447.93526080 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	2
449	450.21046199 ms		Read TxFFE AT Cmd	05	08					
450	450.56758713 ms	Read TxFFE AT Resp (LEN=4)		04	04	Done	Done	Active	Active	C
451	451.32344358 ms		LT_Rsvd (Primary Lane)							
452	451.37764077 ms		LT_Rsvd (Subordinate Lane)							

Figure 8. LT_Resume trigger event



Protocol 1 Listing : USB 4.0 Gen 2-3

Packets

Index	Time	FEC	Channel 1 - 3: USB4 Packet	Channel 2 - 4: USB4 Packet
1	-21.45738022 µs			SLOS1 (Gen2,3)
2	-21.35472401 µs			SLOS1 (Gen2,3)
3	-21.25207234 µs			SLOS1 (Gen2,3)
4	-21.14942702 µs			SLOS1 (Gen2,3)
5	-21.04678574 µs			SLOS1 (Gen2,3)
6	-20.94414634 µs			SLOS1 (Gen2,3)
7	-20.84150947 µs			SLOS1 (Gen2,3)
8	-20.73887607 µs			SLOS1 (Gen2,3)
9	-20.63624743 µs			SLOS1 (Gen2,3)
10	-20.53362149 µs			SLOS1 (Gen2,3)
11	-20.43099802 µs			SLOS1 (Gen2,3)
12	-20.32838107 µs			SLOS1 (Gen2,3)
13	-20.22576728 µs			SLOS1 (Gen2,3)
14	-20.12315457 µs			SLOS1 (Gen2,3)
15	-20.02054645 µs			SLOS1 (Gen2,3)
16	-19.91794180 µs			SLOS1 (Gen2,3)

Figure 9. High-speed lane common-mode voltage

TxFFE Negotiation with the Training.LOCK1 State

The Training.LOCK1 state continues until RxLocked (L0) and RxLocked (L1) are complete. During this state, negotiation for the critical TxFFE settings takes place, and the USB4 high-speed lanes send the high transition density SLOS1 pattern (Figure 10). You can capture this event by triggering on the Rx Active packet as shown in Figure 11.

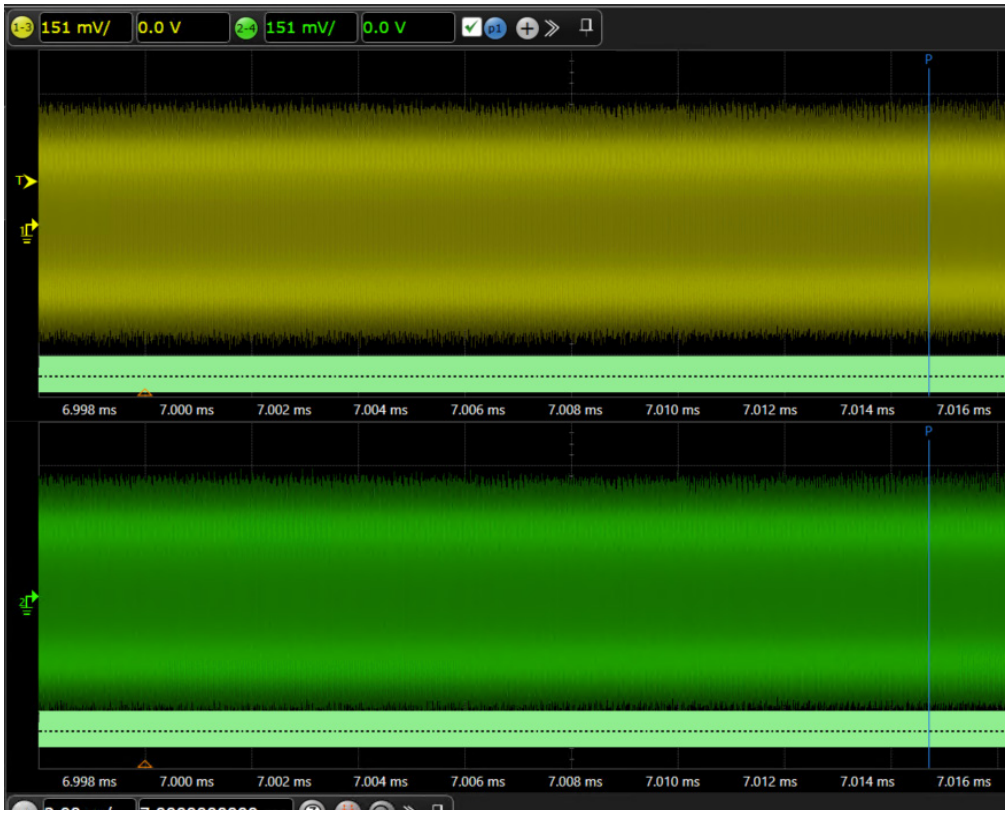


Figure 10. High transition density SLOS1

Protocol 1 Listing : USB4 Low-Speed

Packets

Index	Time	Channel 1: USB4 Low-Speed Pa	Channel 2: USB4 Low-Speed	STX	LEN	Rx Locked (L0	Rx Locked (L1)	Rx Active (L0)	Rx Active (L1	TxF
39	49.76367528 ms		LT_Resume (Primary Lane)							
40	49.81131591 ms		LT_Resume (Subordinate Lane							
41	49.90873276 ms	LT_Resume (Primary Lane)								
42	49.95961305 ms	LT_Resume (Subordinate Lane)								
43	50.68022884 ms	Read TxFFE AT Cmd		05	04					
44	51.03977325 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	0
45	52.89881399 ms		Read TxFFE AT Cmd	05	08					
46	53.11747003 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Inactive	Inactive	2
47	54.60703327 ms	Read TxFFE AT Cmd		05	04					
48	55.13406800 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	2
49	56.61126965 ms		Read TxFFE AT Cmd	05	08					
50	57.05829335 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Inactive	Inactive	2
51	58.54997785 ms	Read TxFFE AT Cmd		05	04					
52	58.86704332 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	2
53	60.74145267 ms		Read TxFFE AT Cmd	05	08					
54	60.98557930 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
55	62.47424347 ms	Read TxFFE AT Cmd		05	04					
56	62.98060195 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Inactive	Inactive	2
57	64.45781666 ms		Read TxFFE AT Cmd	05	08					
58	64.58153368 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2
59	66.39864613 ms	Read TxFFE AT Cmd		05	04					
60	66.69809967 ms		Read TxFFE AT Resp (LEN=4)	04	04	Not Done	Not Done	Active	Inactive	2
61	68.17532098 ms		Read TxFFE AT Cmd	05	08					
62	68.50600408 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	2

Figure 11. Triggering on the Rx Active packet

Completing the TxFFE Negotiation

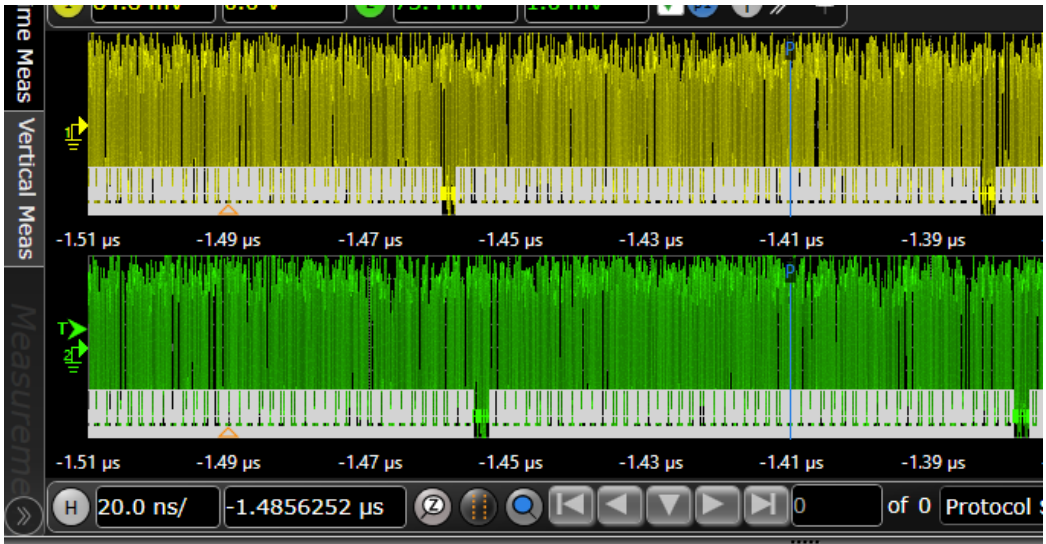
The TxFFE negotiation completes when the RxRequest is set to 0b (Figure 12), and RxLocked (L0) and RxLocked (L1) in the TxFFE register Rx status word are set to 1b “Done”. During this time the transport layer ensures the high-speed lanes will have a continuous stream of idle packets (Figure 13).

Protocol 1 Listing : USB4 Low-Speed

Packets

Index	Time	Channel 1: USB4 Low-Speed Pa	Channel 2: USB4 Low-Speed	STX	LEN	Rx Locked (L0	Rx Locked (L1)	Rx Active (L0)	Rx Active (L1	TxF
411	411.80674142 ms	Read TxFFE AT Cmd		05	04					
412	412.37878426 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
413	415.05185925 ms		Read TxFFE AT Cmd	05	08					
414	415.22856447 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
415	415.73207902 ms	Read TxFFE AT Cmd		05	04					
416	416.10088598 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
417	418.77395661 ms		Read TxFFE AT Cmd	05	08					
418	419.15382310 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
419	419.65733257 ms	Read TxFFE AT Cmd		05	04					
420	420.23752188 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
421	422.91060714 ms		Read TxFFE AT Cmd	05	08					
422	423.08242692 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
423	423.91443272 ms	Read TxFFE AT Cmd		05	04					
424	424.35754070 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
425	426.63272050 ms		Read TxFFE AT Cmd	05	08					
426	427.00756688 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
427	427.83957689 ms	Read TxFFE AT Cmd		05	04					
428	428.09628115 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
429	430.76935887 ms		Read TxFFE AT Cmd	05	08					
430	430.93282988 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
431	431.76484475 ms	Read TxFFE AT Cmd		05	04					
432	432.21627880 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
433	434.49147116 ms		Read TxFFE AT Cmd	05	08					
434	434.86783123 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
435	435.69984575 ms	Read TxFFE AT Cmd		05	04					
436	435.95503539 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
437	438.62811157 ms		Read TxFFE AT Cmd	05	08					
438	438.79303256 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
439	439.62504539 ms	Read TxFFE AT Cmd		05	04					
440	440.07506033 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
441	442.35024563 ms		Read TxFFE AT Cmd	05	08					
442	442.71834669 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
443	443.55035766 ms	Read TxFFE AT Cmd		05	04					
444	443.81427899 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
445	446.48737998 ms		Read TxFFE AT Cmd	05	08					
446	446.64898624 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
447	447.48276719 ms	Read TxFFE AT Cmd		05	04					
448	447.93526080 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	2
449	450.21046199 ms		Read TxFFE AT Cmd	05	08					
450	450.56758713 ms	Read TxFFE AT Resp (LEN=4)		04	04	Done	Done	Active	Active	C
451	451.32344358 ms		LT_Rsvd (Primary Lane)							
452	451.37764077 ms		LT_Rsvd (Subordinate Lane)							

Figure 12. TxFFE register Rx status word



Protocol 1 Listing : USB4 Gen 2-3

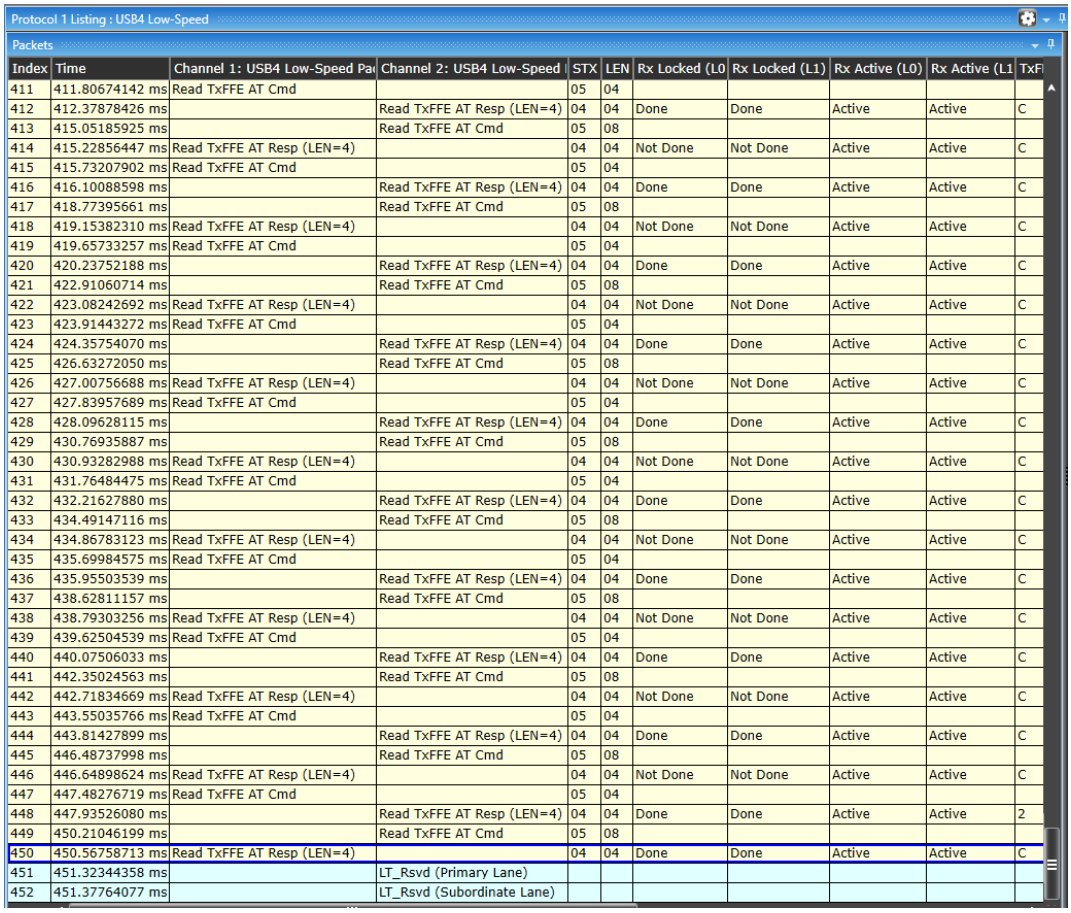
Packets

Index	Time	FEC	Channel 1: USB4 Packet	Channel 2: USB4 Packet	HEC	Length	HopID	SuppID
251	-1.406426149 µs		Idle Packet (Gen2,3)					
252	-1.404887612 µs			Idle Packet (Gen2,3)				
253	-1.404872976 µs		Idle Packet (Gen2,3)					
254	-1.403334341 µs			Idle Packet (Gen2,3)				
255	-1.403319703 µs		Idle Packet (Gen2,3)					
256	-1.401781047 µs			Idle Packet (Gen2,3)				
257	-1.401766358 µs		Idle Packet (Gen2,3)					
258	-1.400227656 µs			Idle Packet (Gen2,3)				
259	-1.400212958 µs		Idle Packet (Gen2,3)					
260	-1.398674357 µs			Idle Packet (Gen2,3)				
261	-1.398659660 µs		Idle Packet (Gen2,3)					
262	-1.397121052 µs			Idle Packet (Gen2,3)				
263	-1.397106348 µs		Idle Packet (Gen2,3)					
264	-1.395567690 µs			Idle Packet (Gen2,3)				
265	-1.395553039 µs		Idle Packet (Gen2,3)					
266	-1.394014239 µs			Idle Packet (Gen2,3)				
267	-1.393999787 µs		Idle Packet (Gen2,3)					
268	-1.392460980 µs			Idle Packet (Gen2,3)				
269	-1.392446487 µs		Idle Packet (Gen2,3)					
270	-1.390907576 µs			Idle Packet (Gen2,3)				
271	-1.390893102 µs		Idle Packet (Gen2,3)					
272	-1.389354154 µs			Idle Packet (Gen2,3)				
273	-1.389339761 µs		Idle Packet (Gen2,3)					
274	-1.387800775 µs			Idle Packet (Gen2,3)				
275	-1.387786440 µs		Idle Packet (Gen2,3)					
276	-1.386247371 µs			Idle Packet (Gen2,3)				

Figure 13. Stream of idle packets on high-speed lanes

Lane Bonding State

The bonding of two single-lane links into a dual-lane link starts when the TS2 ordered sets are transmitted to an adapter in the CL0 state. To ensure the lanes have proper skew, the de-skew ordered set transmits after the TS2 ordered sets. Transmission of the de-skew ordered sets ends the transmission of the TS2 ordered sets. TxFFE concludes on both lanes and RxLocked (L1) is set to “Done” (Figure 14). You can see the high-speed lane transitions from TS2 ordered sets to the de-skew ordered sets in Figure 15.

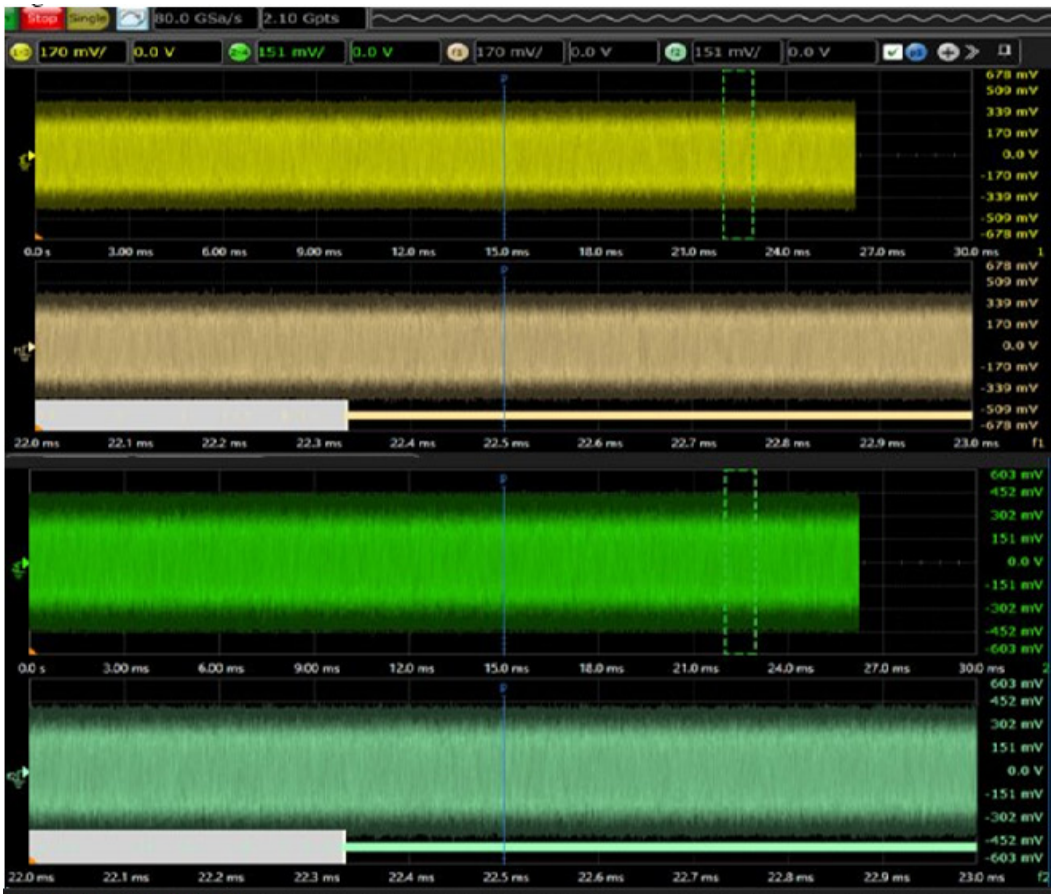


Protocol 1 Listing : USB4 Low-Speed

Packets

Index	Time	Channel 1: USB4 Low-Speed Pa	Channel 2: USB4 Low-Speed	STX	LEN	Rx Locked (L0	Rx Locked (L1)	Rx Active (L0)	Rx Active (L1	TxFI
411	411.80674142 ms	Read TxFFE AT Cmd		05	04					
412	412.37878426 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
413	415.05185925 ms		Read TxFFE AT Cmd	05	08					
414	415.22856447 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
415	415.73207902 ms	Read TxFFE AT Cmd		05	04					
416	416.10088598 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
417	418.77395661 ms		Read TxFFE AT Cmd	05	08					
418	419.15382310 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
419	419.65733257 ms	Read TxFFE AT Cmd		05	04					
420	420.23752188 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
421	422.91060714 ms		Read TxFFE AT Cmd	05	08					
422	423.08242692 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
423	423.91443272 ms	Read TxFFE AT Cmd		05	04					
424	424.35754070 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
425	426.63272050 ms		Read TxFFE AT Cmd	05	08					
426	427.00756688 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
427	427.83957689 ms	Read TxFFE AT Cmd		05	04					
428	428.09628115 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
429	430.76935887 ms		Read TxFFE AT Cmd	05	08					
430	430.93282988 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
431	431.76484475 ms	Read TxFFE AT Cmd		05	04					
432	432.21627880 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
433	434.49147116 ms		Read TxFFE AT Cmd	05	08					
434	434.86783123 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
435	435.69984575 ms	Read TxFFE AT Cmd		05	04					
436	435.95503539 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
437	438.62811157 ms		Read TxFFE AT Cmd	05	08					
438	438.79303256 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
439	439.62504539 ms	Read TxFFE AT Cmd		05	04					
440	440.07506033 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
441	442.35024563 ms		Read TxFFE AT Cmd	05	08					
442	442.71834669 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
443	443.55035766 ms	Read TxFFE AT Cmd		05	04					
444	443.81427899 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	C
445	446.48737998 ms		Read TxFFE AT Cmd	05	08					
446	446.64898624 ms	Read TxFFE AT Resp (LEN=4)		04	04	Not Done	Not Done	Active	Active	C
447	447.48276719 ms	Read TxFFE AT Cmd		05	04					
448	447.93526080 ms		Read TxFFE AT Resp (LEN=4)	04	04	Done	Done	Active	Active	2
449	450.21046199 ms		Read TxFFE AT Cmd	05	08					
450	450.56758713 ms	Read TxFFE AT Resp (LEN=4)		04	04	Done	Done	Active	Active	C
451	451.32344358 ms		LT_Rsvd (Primary Lane)							
452	451.37764077 ms		LT_Rsvd (Subordinate Lane)							

Figure 14. RxLocked (L1) set to “Done”



Packets

Index	Time	FEC	F1:Gate(Ch1): USB4 Packet	F2:Gate(Ch2): USB4 Packet	HEC	Length	HopID	SuppID
413142	22.3326915790779 ms		TS2 (Gen2,3)					
413143	22.3326916156164 ms			TS2 (Gen2,3)				
413144	22.3326946914741 ms		TS2 (Gen2,3)					
413145	22.3326947280766 ms			TS2 (Gen2,3)				
413146	22.3326978038362 ms		TS2 (Gen2,3)					
413147	22.3326978405176 ms			TS2 (Gen2,3)				
413148	22.3327009163457 ms		TS2 (Gen2,3)					
413149	22.3327009530818 ms			TS2 (Gen2,3)				
413150	22.3327040286865 ms		TS2 (Gen2,3)					
413151	22.3327040654631 ms			TS2 (Gen2,3)				
413152	22.3327071410437 ms		TS2 (Gen2,3)					
413153	22.3327071777677 ms			TS2 (Gen2,3)				
413154	22.3327102534327 ms		TS2 (Gen2,3)					
413155	22.3327102901695 ms			TS2 (Gen2,3)				
413156	22.3327133658128 ms		De-Skew (Gen2,3)					
413157	22.3327134024686 ms			De-Skew (Gen2,3)				
413158	22.3327164780455 ms		De-Skew (Gen2,3)					
413159	22.3327165148708 ms			De-Skew (Gen2,3)				

Figure 15. Tx and Rx line transitions from TS2 ordered sets to de-skew ordered sets

Link Partner Disconnect and System Sleep State

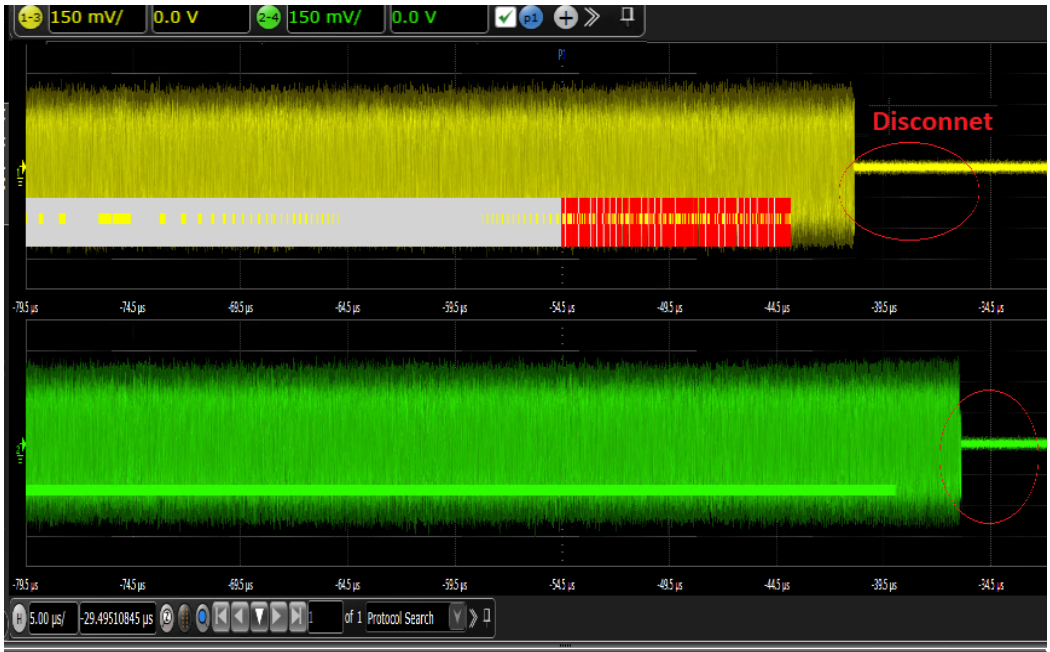
When link partners disconnect, it is important to ensure the DUT enters the System Sleep state. You can achieve this by sending the LT_LRoff Transaction (Figure 16) and confirm it when the Tx and Rx lines become inactive (Figure 17).

Protocol 1 Listing : USB 4.0 Low-Speed

Packets

Index	Time	Channel 1: USB4 Low-Speed Packet	Channel 2: USB4 Low-Speed Packet	STX	LEN	Rx Locked (L0)	Rx Locked (L1)
1	-18.2896 µs	LT_LRoff (Primary Lane)					
2	935.9952 µs		LT_LRoff (Primary Lane)				

Figure 16. LT_LRoff transaction packet



Protocol 1 Listing : USB 4.0 Gen 2-3

Packets

Index	Time	FEC	USB4 Packet	HEC	Length	HopID	SuppID	PDF	Sequence Number	Address	Data	CRC
97033	-54.50407465 µs		Idle Packet (Gen2,3)									
97034	-54.50329709 µs		Idle Packet (Gen2,3)									
97035	-54.50251944 µs		Idle Packet (Gen2,3)									
97036	-54.50174185 µs		Idle Packet (Gen2,3)									
97037	-54.50096422 µs		Idle Packet (Gen2,3)									
97038	-54.50018660 µs		Idle Packet (Gen2,3)									
97039	-54.49940895 µs		Idle Packet (Gen2,3)									
97040	-54.49863133 µs		Idle Packet (Gen2,3)									
97041	-54.49785372 µs		Idle Packet (Gen2,3)									
97042	-54.49707612 µs		Idle Packet (Gen2,3)									
97043	-54.49629854 µs		Idle Packet (Gen2,3)									
97044	-54.49552091 µs		Idle Packet (Gen2,3)									
97045	-54.49474331 µs		Unknown Packet									
97046	-54.49163282 µs		Unknown Packet									
97047	-54.48852231 µs		Unknown Packet									
97048	-54.45722343 µs		Unknown Packet									

Figure 17. UXR oscilloscope displays inactive Tx and Rx lines

Summary

Bringing up a Type-C link is a complex task due to the numerous Type-C, USB-PD, and high-speed negotiations and requirements defined by each standard. Therefore, it is critical to ensure all Type-C technologies communicate correctly particularly with USB4. The USB4 link is complicated due to several factors which include the 20 Gbps signaling rate, crosstalk from three other lanes running at the same speed, a bonded aggregate bit rate of 40 Gbps, and the need for optimization over a low-cost passive cable.

This application note uses USB4 to demonstrate the tools to debug and optimize a Type-C link. This is accomplished by connecting to a DUT, triggering on low-speed packets, capturing/decoding sideband and high-speed signals, and viewing the time-correlated waveforms to determine potential signal integrity issues.

For More Information

- Keysight USB Type-C Connectivity Solution Guide
- USB-PD Specification
- USB Type-C Cable and Connector Specification