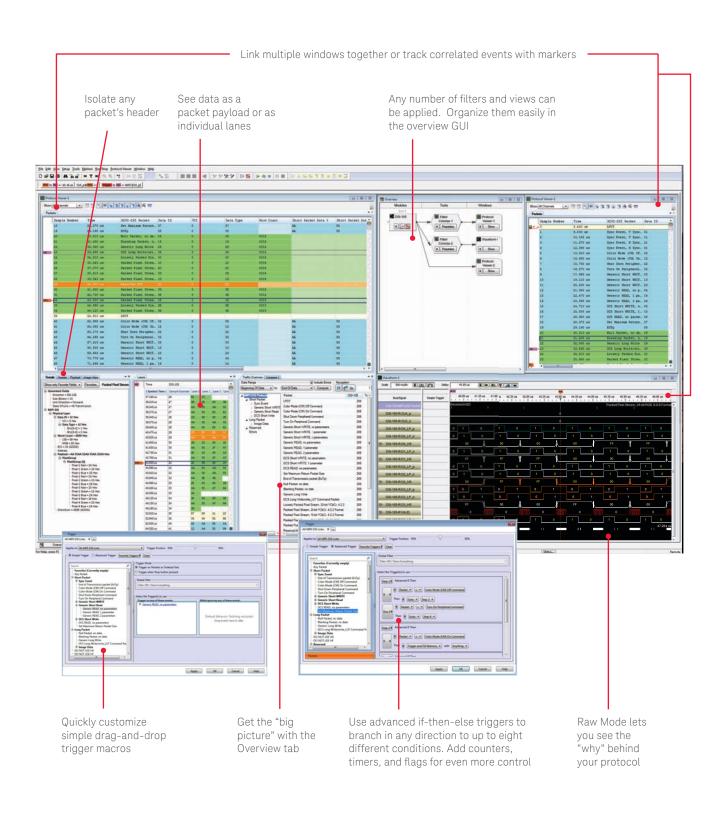
## Keysight Technologies U4421A MIPI® D-PHY<sup>™</sup> Protocol Exerciser/Analyzer





# The MIPI D-PHY Analyzer, Two Instruments in One (Available with Option 601 or 603)



### The MIPI D-PHY Analyzer, Two Instruments in One (Available with Option 601 or 603) (continued)

## The U4421A MIPI D-PHY Analyzer option for CSI-2 and DSI gives you deep insight into your mobile computing designs

Time correlate multiple busses and views. Multiple modules (D-PHY, PCI, DDR, high-speed logic, and HDMI) can be installed in one mainframe, and multiple frames can be connected. Any number of filters and views can be applied. Organize them easily in the overview GUI. Link multiple windows together or track correlated events with markers.

Look deeply into packets with "peel off" tabs. Isolate any packet's header, or data as a packet payload or individual lanes.

Raw Mode lets you see the "why" behind your protocol. Raw state data that is acquired by the analyzer can be displayed as a time-correlated waveform view.

Get the "big picture" with the Overview tab. Get a count of the various types of traffic in any period of time, including errors; then step through each occurrence with embedded navigation tools.

Isolate events with protocol-aware triggers. Simple drag-and-drop trigger macros can be quickly customized. Or use advanced if-then-else triggers to branch in any direction to up to eight different conditions. Trigger on packet types, errors or into payload data.

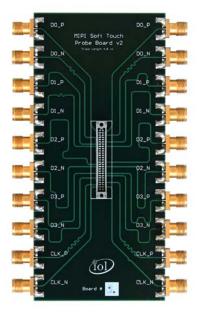
Probe any system with three flexible probing options (below). The E5381A differential flying leads let you connect to vias, headers, and traces. The E5404A Soft Touch Pro probe gives you a rugged in-board connection to a small footprint. In addition, UNH-IOL has created an SMA to Soft Touch break-out board that connects directly to their Reference Termination Board, or be used as a generic mid-bus adapter.

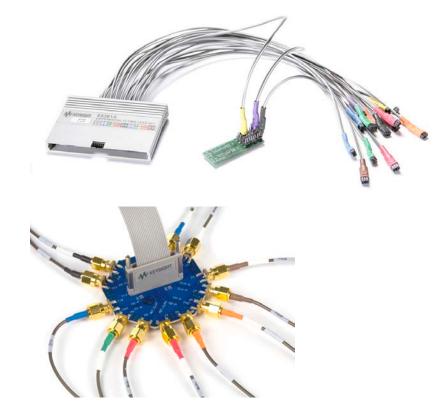
### Key features:

- Protocol aware for DSI and CSI-2 traffic in all views, triggers, and filters
- Up to 1.5 Gb data rate
- Up to 16 GB Trace Depth
- Up to 4 data lanes + CLK
- 5-ns resolution raw mode data
- N-way trigger branching
- Integrated image extraction software

## Target users: Designers and validators of

- Mobile devices
- Mobile embedded systems
- MIPI silicon/IP
- Cameras





## The MIPI D-PHY Analyzer, Two Instruments in One (Available with Option 601 or 603) (continued)

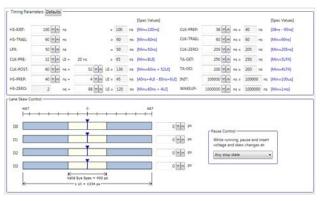
## The U4421A MIPI D-PHY Analyzer option for CSI-2 and DSI gives you deep insight into your mobile computing designs (continued)

	File Name		Size		File Pa
0	720p loop.csv		21.26 MB	C/Users\DDS-U4421	A-DEMO
0	godzilla.csv	<u>i</u>	69.40 MB	CAUsers\DDS-U4421	A-DEMO
•	Tri color.csv	2	492.88 KB	C\Users\DDS-U4421	A-DEMC
) Ne	m w File ) 💠 Add To List	X Remove	Add To Run Sequen	ce.	,
	luence	File		Loop Count	1
godzil	la.csv			1 .	٠
720p	loop.ctv			Loop Forever *	٠
					×
tal M	emory Used: 45.23 MB (Ma	x. 8.00 GB)			
	ad Sequence		-		
				and the second se	Ciricel

End-to-end data path analysis: Quickly create exerciser traffic ...

onnection Setup	Analyzer Setup	Exerciser Electrical	Exerciser Timing	Exerciser Data	Packet Insertion
Errors		t Checksum value to			New
Processing		ced where "Special"			Edit
Bad ECC Processing		t an ECC value of 11 I where Special Inser			A Move Up
Color Mc					Move Down
Processing.	DSI Color Mode	On command			
Color Mc Processing.	DSI Color Mode	Off command			
Cancel Rea	idy				

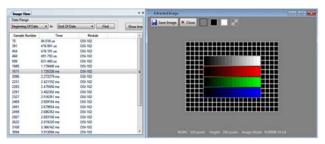
... or inserted packets...



Adjust timing parameters, including data rate, output voltage, skew rate, signal timing, and lane skew.

Pixel Stream Mode Packed Pixel Stream, 24-bit I	RGB 8-8-8 Format		L1: VSA	T1	BLLP			
L3 (VACT lines)	Horizontal Active Pixel	Count	Lines	LP	11 or Blanki			
720 0	1260		Lines		C1			
Link Width	HS Bit Rate (Mbps)		LE VACT				1	
*x1 0x2 0x3 0x4	750		Lines	HBP	Pixel	BLLP-2 + HEP		
L1 (VSA linet)	L2 (VBP lines)			LP-11 or Dianking	Stream	LP-11 or Blanking Packet		
2 20	2 20			Packet	(Burst)	1000720		
L4 (VFP lines)	Clock enable time befo	ve Parket (ns)		a		4		
2 2 0	100 9	ALL ACALL POP	L4: VEP Lines	UP	BLLP.		1	
T1: Line time (ns)	Virtual Channel		Lines		C1	and the second s		
			N	Vext Frame	VSS.	Sync Event, V-Sync	Start	
41066.67 Oxford frame count	0		N	Vext Frame	NSS:	Sync Event, H-Sync	Stat	
41066.67 Output frame count				Vext Frame	HSS		Start	
Output frame count 2 BLIP-1	0		Image Selection	Hext Frame	HSS	Sync Event, H-Sync 1.C2.C3 : Byte Court	Start	
Output frame count 2 BLIP-1 C1 (Byte	0 YA		Image Selection	File Path	Calc	Sync Event, H-Sync (1,C2,C3 : Byte Cour lated from Bit Rate (1	Start t Mbs) Height	
Output frame count 2 BLIP-1	0		Image Selection	File Path MO-1\Deskto	Calco	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	1280
Output frame count 2 BLIP-1 Elanking 8LIP-2 + MF8	0 m (ns) 42024		Image Selection	File Path MO-1\Deskto	Calco	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	
Output frame count 2 BLLP-1 Elanking • 3840 BLLP-2 + HF8 C2 (Byte	Count) Count) Time (ns) 41024 Count) Time		Image Selection	File Path MO-1\Deskto	Calco	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	1280
Output frame count 2 BLIP-1 Elanking BLIP-2 + HFB C2 (Byte Blanking 0	0 m (ns) 42024	8-+	Image Selection	File Path MO-1\Deskto	Calco	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	1280
Output frame count 2 BLLP-1 C1 (Byte Blanking • 3840 BLLP-2 + HFB C2 (Byte Blanking • 0 HBP	Count) Time (ns) 41024 Count) Time		Image Selection	File Path MO-1\Deskto	Calco	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	1280
Output frame count 2 BLIP-1 C1 (Byte Blanking • 3840 BLIP-2 + HFB C2 (Byte Blanking • 0 HBP C3 (Byte	Count) Time (nn) 41024 Count) Time Count) Time Count) Time	8(-)+)	Image Selection	File Path MO-1\Deskto	Calco	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	1280
Output frame count 2 BLIP-1 C1 (Byte Blanking • 3840 BLIP-2 + HFB C2 (Byte Blanking • 0 HBP C3 (Byte	Count) Time (ns) 41024 Count) Time		Image Selection	File Path MO-1\Deskto	Calco Calco Op/BMP/Fra	Sync Event, H-Sync (1,C2,C3): Byte Courr lated from Bit Rate (1 me 1 - bars - 720p.	Start t Mbs) Height 720	1280

... based on images or commands ...



... analyze and extract the transmitted images by physically probing or using the analyzer's internal loopback.

## The MIPI D-PHY Analyzer, Two Instruments in One (Available with Option 601 or 603) (continued)

## The U4421A MIPI D-PHY Analyzer option for CSI-2 and DSI gives you deep insight into your mobile computing designs (continued)

The U4421A MIPI D-PHY Exerciser option for CSI-2 and DSI provides the record depth necessary to stimulate designs with high-definition images and video. It also lets you simulate traffic from a wide variety of devices busses of varying signal performance.

Deep memory. With 1GB of standard memory, and with options for 4 GB and 16 GB, you can generate long sequences of high definition images and videos.

Internal loopback, available with the U4421A analyzer Options 601 and 603, lets you verify the exerciser's output. This gives you additional confidence in the data that you are sending to your target.

Change both HP and LP signal levels to understand how your system reacts to diminished signal voltages. A system that can tolerate lower signal swings will usually have a longer battery life.

Change signal data rate, slew rate, and lane timing to get insight into how your systems and peripherals react to a wide variety of CSI and DSI signals. Bring the "plug-fest" experience to your bench.

Generate traffic quickly with your own CSV files, the integrated packet inserter or the optional image inserter software. Recall your favorite patterns with user-defined "hot" (shortcut) keys.

Each module can simultaneously be an exerciser and an analyzer. Combine multiple modules in a 2 (M9502A) or 5 (M9505A) slot AXIe mainframe to analyze and simulate cross-system behavior.



### Key features:

- Generate user-defined D-PHY traffic
- Up to 1.5 GB data rate
- Up to 16 GB trace depth
- Change speed, slew rate, voltage levels and lane skew
- Flexible pattern creation
  GUI
  - Packet inserter
  - Image inserter

## Target users: Designers and validators of

- Mobile devices
- Mobile embedded systems
- MIPI silicon/IP
- Displays

## Keysight U4421A – Analyzer Option (601) Performance Characteristics

Electrical	
HSV minimum differential	100 mV
LPV threshold range	0 to 1.5 V
Lane width	Up to 4 with Option 004. Analyze 1-, 2-, 3-, or 4-lane systems
Performance	
Maximum bit rate (high-speed mode)	1.5 Gbps
Minimum bit rate (high-speed mode)	80 Mbps
Maximum bit rate (low-power mode)	10 Mbps
Minimum bit rate (low-power mode)	N/A
Raw mode LP sample resolution	5 ns, typical for LP traffic; 1 ÷ bit rate for HS traffic
Maximum data rate of probes E5381A	1.5 Gbps with 82 $\Omega$ coaxial resistor adapter, 1.0 Gbs with damped wire and 3-pin header adapters.
E5405A	1.5 Gbps
Memory	User allocated (shared among exerciser, analyzer and raw mode)
Standard Option M04 (recommended for images) Option M16 (recommended for video)	1 GB 4 GB 16 GB
Protocol Protocol version support	
Display	Display Serial Interface (DSI) v1.1 Display Serial Interface (DSI) v1.02.00 Display Serial Interface Version 1.01.00 Display Command Set (DCS) v1.1 Display Command Set (DCS) v1.02.00 Display Command Set v1.01.00 Stereoscopic Display Formats (SDF) v1.0
Camera (CSI-2)	Camera Serial Interface 2 v1.01.00 Camera Serial Interface 2 v1.00 (CSI-2)
Protocol viewer	Hierarchical packet-level display
Protocol views	Packets, header, lanes, payload, and traffic overview
Protocol decoder	
Simultaneous HS and LP data support	Yes
Short and long packet decode	Yes
CSI-2 and DSI-1 decode	Yes, user selectable
Waveform view (Raw Mode)	Packets and lanes
Error display	
SOT error display	Yes
EOT error display	Yes
Escape error display	Yes
Sequence error display	Yes
Turnaround error display	Yes
ECC, CRC error display	Yes
Contention detection	No
Track changes in speed (HS/LP) mode	Yes
Correlation markers	> 1,000 user-defined
Marker measurements	Yes, user-defined time and count measurements
Window correlation lock	Yes, user-defined

### Keysight U4421A – Analyzer Option (601) Performance Characteristics (Continued)

Triggering capabilities	
Trigger on protocol commands	Yes, with > 130 macros
Simple trigger	Drag and drop
Advanced trigger	
Sequence levels	Up to 8
Logical branching	N-way
Trigger on protocol patterns	Yes, on both DSI and CSI long and short packet headers
Protocol pattern customization	Yes, with bit-level editing
Payload pattern matcher	First 4 bytes
Event counter	Yes
Time counter	Yes, 100 ns accuracy
Real-time error detection	5 ns resolution ± 5 ns of accuracy
SOT error trigger	Yes, on a per lane basis
EOT error trigger	Yes, on a per lane basis
Escape error trigger	Yes, on a per lane basis
Sequence error trigger	Yes, on a per lane basis
Turnaround error trigger	Yes, on a per lane basis
ECC	Yes
CRC	Yes
Display	
Low power state of data transmission	All escape mode actions, except ultra-low power
Stopped	No
Image extractor / Image inserter	
DSI	
Burst mode	Packed pixel stream, 16-bit RGB, 5-6-5 format
	Packed pixel stream, 18-bit RGB, 6-6-6 format
	Loosely packed pixel stream, 18-bit RGB, 6-6-6 format
	Packed pixel stream, 24-bit RGB, 8-8-8 format
	Packed pixel stream, 30-bit RGB, 10-10-10 format
	Packed pixel stream, 36-bit RGB, 12-12-12 format
	Packed pixel stream, 12-bit YCbCr, 4:2:0 format
	Packed pixel stream, 16-bit YCbCr, 4:2:2 format
	Loosely packed pixel stream, 20-bit YCbCr, 4:2:2 format
	Packed pixel stream, 24-bit YCbCr, 4:2:2 Format
Non-burst mode	Packed pixel stream, 16-bit RGB, 5-6-5 format
	Packed pixel stream, 18-bit RGB, 6-6-6 format
	Loosely packed pixel stream, 18-bit RGB, 6-6-6 format
	Packed pixel stream, 24-bit RGB, 8-8-8 format
	Packed pixel stream, 30-bit RGB, 10-10-10 format
	Packed pixel stream, 36-bit RGB, 12-12-12 format
	Packed pixel stream, 12-bit YCbCr, 4:2:0 format
	Packed pixel stream, 16-bit YCbCr, 4:2:2 format
	Loosely packed pixel stream, 20-bit YCbCr, 4:2:2 format
	Packed pixel stream, 24-bit YCbCr, 4:2:2 format
Command mode	3 bits per pixel
	8 bits per pixel
	12 bits per pixel
	16 bits per pixel
	18 bits per pixel
	24 bits per pixel

## Keysight U4421A – Analyzer Option (601) Performance Characteristics (Continued)

Image extractor / Image inserter (Continued)	
CSI	
	RGB444
	RGB555
	RGB565
	RGB666
	RGB888
	YUV420 8-bit
	YUV420 8-bit (Chroma shifted pixel sampling) legacy YUV420 8-bit
	YUV420 10-bit
	YUV420 10-bit (Chroma shifted pixel sampling) YUV422 8-bit
	YUV422 10-bit
	RAW6
	RAW7
	RAW8
	RAW10
	RAW12
	RAW14

## Keysight U4421A – Analyzer Option (602) Performance Characteristics

Lane width    Up to 4 with Option 404. Exercise 1-, 2-, 3-, or 4-lane systems      Low-power voltage ling adjustment    ± 100 MV      Lew-power voltage ling adjustment    ± 100 MV      High-speed common mode voltage    60 mV to 320 mV      Uptu d'riving impedance    High-speed. 50 Q. Low-power: 82.4 Q      Bus termination modes    Open, dynamic, static 100 0 d'ifferential      Waveform timing control    Yes, automatic or manual settings      CLK-POST timing control    Yes, automatic or manual settings      CLK-PER timing control    Yes, automatic or manual settings      CLK-PER Thring control    Yes, automatic or manual settings      CLK-ZENO timing control    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-TRAIL    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      LPX<	Electrical	Features
Low-power voltage low adjustment    ± 100 mV      High-speed output differential voltage    60 mV to 380 mV      Dutput driving impedance    High-speed common mode voltage      Bus termination modes    Open, dynamic, static 100 Outfferential      Waveform timing control    Yes, automatic or manual settings      CLK-POST timing control    Yes, automatic or manual settings      CLK-PRE timing control    Yes, automatic or manual settings      CLK-PRE Training control    Yes, automatic or manual settings      CLK-TRAL timing control    Yes, automatic or manual settings      HS-PEPARE    Yes, automatic or manual settings      HS-PEPARE    Yes, automatic or manual settings      HS-ZERO    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_GO    Yes, automatic or manual settings      TA_GO    Yes, automatic or manual settings      TA_GO    Yes, automatic or manual settings      CLK ZERO Nipe    Yes, automatic or manual settings      TA_GO <td< td=""><td>Lane width</td><td>Up to 4 with Option 404. Exercise 1-, 2-, 3-, or 4-lane systems</td></td<>	Lane width	Up to 4 with Option 404. Exercise 1-, 2-, 3-, or 4-lane systems
High-speed common mode voltage  60 mV to 320 mV    High-speed common mode voltage  60 mV to 380 mV    Output driving impedance  High-speed 50 Ω; Low-power: 82.4 Ω    Bus termination modes  Open, dynamic, static 100 0 differential    Wavform timing control  Yes, automatic or manual settings    CLK-POST timing control  Yes, automatic or manual settings    CLK-PRE PARE timing control  Yes, automatic or manual settings    CLK-TRED timing control  Yes, automatic or manual settings    CLK-TRED timing control  Yes, automatic or manual settings    CLK-TRED timing control  Yes, automatic or manual settings    CLK-TERO timing control  Yes, automatic or manual settings    HS-EXIT timing control  Yes, automatic or manual settings    HS-FEFARE  Yes, automatic or manual settings    HS-FEFARE  Yes, automatic or manual settings    LPX  Yes, automatic or manual settings    LPX  Yes, automatic or manual settings    TA_GO  Yes, automatic or manual settings    CLK lane and data lane skew adjust  5 ps, resolution typical; ± 0.5 Ul @ 1 GB and above    Reference clock input  Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB    Performance  Maximum bit rate (high-speed mode)    Mainimum bit rate (high-speed mode)  800 Kbps    Minimum bit	Low-power voltage high adjustment	500 mV to 1.5 V
High-speed common mode voltage    60 mV to 380 mV      Output driving impedance    High-speed 50 Q, Low-power: 82.4 Q      Bus termination modes    Open, dynamic, static 100 Q differential      Waveform timing control    Yes, automatic or manual settings      CLK-PQST timing control    Yes, automatic or manual settings      CLK-PRE timing control    Yes, automatic or manual settings      CLK-PRE timing control    Yes, automatic or manual settings      CLK-TRAIL timing control    Yes, automatic or manual settings      CLK-ZRD timing control    Yes, automatic or manual settings      HS-EXIT timing control    Yes, automatic or manual settings      HS-TREPARE    Yes, automatic or manual settings      HS-TREPARE    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_G0    Yes, automatic or manual settings      TA_G0    Yes, automatic or manual settings      Reference clock input    Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB      Performace    Maximum bit rate (high-speed mode)    1.5 Gbps      Minimum bit rate (high-speed mode)    1.0 Mbps    Maximum bit rate (low-power mode)    80 Mbps	Low-power voltage low adjustment	± 100 mV
Output driving impedance      High-speed: 50 G; Low-power: 82.4 Q        Bus termination modes      Open, dynamic, static 100 Q differential        Waveform timing control      Yes, automatic or manual settings        CLK-PRS Timing control      Yes, automatic or manual settings        CLK-PRE Timing control      Yes, automatic or manual settings        CLK-PRE Timing control      Yes, automatic or manual settings        CLK-TRAIL timing control      Yes, automatic or manual settings        CLK-TRAIL timing control      Yes, automatic or manual settings        CLK-ZERO timing control      Yes, automatic or manual settings        HS-EXIT timing control      Yes, automatic or manual settings        HS-FEPARE      Yes, automatic or manual settings        HS-TRAIL      Yes, automatic or manual settings        LPX      Yes, automatic or manual settings        TA_Get      Yes, automatic or manual settings        TA_GO      Yes, automatic or manual settings        Maximum bit rate (high-speed mode)      15 Gbps        Mininum bit rate (high-speed mode)      10 Mbps </td <td>High-speed output differential voltage</td> <td>60 mV to 320 mV</td>	High-speed output differential voltage	60 mV to 320 mV
Bus termination modes      Open, dynamic, static 100 Ω differential        Waveform timing control      Yes, automatic or manual settings        CLK-PRET timing control      Yes, automatic or manual settings        CLK-PRETARE timing control      Yes, automatic or manual settings        CLK-PRETARE timing control      Yes, automatic or manual settings        CLK-TRAIL timing control      Yes, automatic or manual settings        CLK-TRAIL timing control      Yes, automatic or manual settings        HS-EXIT timing control      Yes, automatic or manual settings        HS-EXIT timing control      Yes, automatic or manual settings        HS-TRAIL      Yes, automatic or manual settings        HS-TRAIL      Yes, automatic or manual settings        LFX      Yes, automatic or manual settings        TA_Get      Yes, automatic or manual settings        TA_GO      Yes, automatic or manual settings        CLK lane and data lane skew adjust      5 ps, resolution typical; ± 0.5 UI @ 1 GB and above        Reference clock input      Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB        Performance      Maximum bit rate (high-speed mode)        Minimum bit rate (high-speed mode)      1.5 Gbps        Minimum bit rate (low-power mode)      100 Mbps <td>High-speed common mode voltage</td> <td>60 mV to 380 mV</td>	High-speed common mode voltage	60 mV to 380 mV
Waveform timing control  Yes, automatic or manual settings    CLK-PRST timing control  Yes, automatic or manual settings    CLK-PRE timing control  Yes, automatic or manual settings    CLK-PRE timing control  Yes, automatic or manual settings    CLK-REAPARE timing control  Yes, automatic or manual settings    CLK-TRALL timing control  Yes, automatic or manual settings    CLK-ZER0 timing control  Yes, automatic or manual settings    HS-PREPARE  Yes, automatic or manual settings    HS-PREPARE  Yes, automatic or manual settings    HS-TRAIL  Yes, automatic or manual settings    LPX  Yes, automatic or manual settings    LPX  Yes, automatic or manual settings    TA_GO  Yes, automatic or manual settings    TA_GO  Yes, automatic or manual settings    CLK lane and data lane skew adjust  5 ps, resolution typical; ±0.5 U @ 1 GB and above    Reference clock input  Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB    Performance  Maximum bit rate (high-speed mode)    Minimum bit rate (high-speed mode)  1.5 Gbps    Minimum bit rate (high-speed mode)  10 Mbps    Minimum bit rate (high-speed mode)  10 Mbps    Minimum bit rate (high-speed mode)  10 GB    Qption M04 (recommended for images)  4 GB	Output driving impedance	High-speed: 50 $\Omega$ ; Low-power: 82.4 $\Omega$
CLK-POST timing control    Yes, automatic or manual settings      CLK-PRE timing control    Yes, automatic or manual settings      CLK-PREPARE Timing control    Yes, automatic or manual settings      CLK-TRALL timing control    Yes, automatic or manual settings      CLK-TRALL timing control    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-TRAL    Yes, automatic or manual settings      HS-TRAL    Yes, automatic or manual settings      HS-TRAL    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_Get    Yes, automatic or manual settings      TA_GO    Yes, automatic t	Bus termination modes	Open, dynamic, static 100 $\Omega$ differential
CLK-PRE timing control    Yes, automatic or manual settings      CLK-PREPARE timing control    Yes, automatic or manual settings      CLK-ZERO timing control    Yes, automatic or manual settings      CLK-ZERO timing control    Yes, automatic or manual settings      HS-EXIT timing control    Yes, automatic or manual settings      HS-FREARE    Yes, automatic or manual settings      HS-TRAIL    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_G0    Yes, automatic or manual settings      TA_G0    Yes, automatic or manual settings      CLK lane and data lane skew adjust    5 ps, resolution typical; ± 0.5 UI @1 GB and above      Reference clock input    Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB      Performance    Maximum bit rate (high-speed mode)    1.5 Gbps      Minimum bit rate (high-speed mode)    1.0 Mbps    Mode)      Maximum bit rate (low-power mode)    10 Mbps    Maximum bit rate (high-speed mode)      Minimum bit rate (high-speed mode)    1.6 GB    Packet insertion      Mode (recommended for images)    4 GB    0ption M04 (recommended for images)    4 GB      Option M04 (rec	Waveform timing control	Yes, automatic or manual settings
CLK-PREPARE timing control    Yes, automatic or manual settings      CLK-TRAIL timing control    Yes, automatic or manual settings      CLK-ZERO timing control    Yes, automatic or manual settings      HS-EXIT timing control    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-TRAIL    Yes, automatic or manual settings      HS-TRAIL    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_Get    Yes, automatic or manual settings      TA_GO    Yes, automatic or manual settings      Maimum bit rate (high-speed mode)    1.5 Gbps <td>CLK-POST timing control</td> <td>Yes, automatic or manual settings</td>	CLK-POST timing control	Yes, automatic or manual settings
CLK-TRAIL timing control    Yes, automatic or manual settings      CLK-ZERO timing control    Yes, automatic or manual settings      HS-EXIT timing control    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-ZERO    Yes, automatic or manual settings      HS-TRAIL    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_Get    Yes, automatic or manual settings      TA_GO    Yes, automatic or manual settings      CLK lane and data lane skew adjust    5 ps, resolution typical; ± 0.5 UI @ 1 GB and above      Reference clock input    Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB      Performance    Maximum bit rate (high-speed mode)    1.5 Gbps      Minimum bit rate (high-speed mode)    1.5 Gbps    Minimum bit rate (high-speed mode)    80 Mbps      Maximum bit rate (low-power mode)    10 Mbps    Maximum bit rate (low-power mode)    80 Mbps      Maintimum bit rate (low-power mode)    10 Mbps    Maximum bit rate (low-power mode)    80 Mbps      Maximum bit rate (low-power mode)    16 B    Packet insertion    Memory    User allocated (shared among Exerciser, Analyzer and Raw Mode)    Standard    1 GB <t< td=""><td>CLK-PRE timing control</td><td>Yes, automatic or manual settings</td></t<>	CLK-PRE timing control	Yes, automatic or manual settings
CLK-ZERO timing control    Yes, automatic or manual settings      HS-FXIT timing control    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-PREPARE    Yes, automatic or manual settings      HS-TRAIL    Yes, automatic or manual settings      LPX    Yes, automatic or manual settings      TA_Get    Yes, automatic or manual settings      TA_GO    Yes, automatic or manual settings      CLK lane and data lane skew adjust    5 ps, resolution typical; ± 0.5 UI @ 1 GB and above      Reference clock input    Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB      Performance    Waximum bit rate (high-speed mode)      Maximum bit rate (high-speed mode)    1.5 Gbps      Minimum bit rate (low-power mode)    10 Mbps      Maximum bit rate (low-power mode)    800 Kbps      Memory    User allocated (shared among Exerciser, Analyzer and Raw Mode)      Standard    1 GB      Option M04 (recommended for images)    4 GB      Option M16 (recommended for images)    4 GB      Option M16 (recommended for video)    16 GB      Packet insertion    No      HSDT request error generation    Yes, with timing control to violate specs </td <td>CLK-PREPARE timing control</td> <td>Yes, automatic or manual settings</td>	CLK-PREPARE timing control	Yes, automatic or manual settings
HS-EXIT timing controlYes, automatic or manual settingsHS-PREPAREYes, automatic or manual settingsHS-ZEROYes, automatic or manual settingsHS-TRAILYes, automatic or manual settingsLPXYes, automatic or manual settingsTA_GetYes, automatic or manual settingsTA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformance1.5 GbpsMaimum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)10 MbpsMainum bit rate (low-power mode)1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationYes, with operate in slave mode)	CLK-TRAIL timing control	Yes, automatic or manual settings
HS-PREPAREYes, automatic or manual settingsHS-ZEROYes, automatic or manual settingsHS-TRAILYes, automatic or manual settingsLPXYes, automatic or manual settingsTA_GetYes, automatic or manual settingsTA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformanceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMainimum bit rate (low-power mode)10 MbpsMainimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M16 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsSOT synch error generationYes, with timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)No (does not operate in slave mode)No (does not operate in slave mode)	CLK-ZERO timing control	Yes, automatic or manual settings
HS-ZEROYes, automatic or manual settingsHS-TRAILYes, automatic or manual settingsLPXYes, automatic or manual settingsTA_GetYes, automatic or manual settingsTA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformanceMaximum bit rate (high-speed mode)Maximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)10 MbpsMainmum bit rate (low-power mode)10 MbpsMainmum bit rate (low-power mode)10 MbpsMaindrad1 GBOption M04 (recommended for images)4 GBOption M04 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	HS-EXIT timing control	Yes, automatic or manual settings
HS-TRAILYes, automatic or manual settingsLPXYes, automatic or manual settingsTA_GetYes, automatic or manual settingsTA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformaceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMontyUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	HS-PREPARE	Yes, automatic or manual settings
LPXYes, automatic or manual settingsTA_GetYes, automatic or manual settingsTA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformanceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (low-power mode)10 MbpsMaximum bit rate (low-power mode)10 MbpsMainmum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsSOT synch error generationYes, with timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	HS-ZERO	Yes, automatic or manual settings
TA_GetYes, automatic or manual settingsTA_GOYes, automatic or manual settingsTA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformanceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionHSDT request error generationYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	HS-TRAIL	Yes, automatic or manual settings
TA_GOYes, automatic or manual settingsCLK lane and data lane skew adjust5 ps, resolution typical; ± 0.5 UI @ 1 GB and aboveReference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformanceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (low-power mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMaximum bit rate (low-power mode)800 KbpsMaximum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	LPX	Yes, automatic or manual settings
CLK lane and data lane skew adjust    5 ps, resolution typical; ± 0.5 Ul @ 1 GB and above      Reference clock input    Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB      Performance    Maximum bit rate (high-speed mode)    1.5 Gbps      Minimum bit rate (high-speed mode)    80 Mbps    Maximum bit rate (low-power mode)    10 Mbps      Maximum bit rate (low-power mode)    10 Mbps    Momory    User allocated (shared among Exerciser, Analyzer and Raw Mode)      Standard    1 GB    Option M04 (recommended for images)    4 GB      Option M16 (recommended for video)    16 GB    Packet insertion      HSDT request error generation    Yes, with timing control to violate specs    SOT synch error generation      SOT synch error generation    Yes, with timing control to violate specs    LPD transmission error generation      LPD transmission error generation    Yes, with waveform timing control and direct control of data transmitted on the link      Protocol errors    Yes    Yes      Turnaround error generation    No (does not operate in slave mode)	TA_Get	Yes, automatic or manual settings
Reference clock inputRequired, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MBPerformanceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	TA_GO	Yes, automatic or manual settings
PerformanceMaximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsSOT synch error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	CLK lane and data lane skew adjust	5 ps, resolution typical; ± 0.5 UI @ 1 GB and above
Maximum bit rate (high-speed mode)1.5 GbpsMinimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionHSDT request error generationYes, with timing control to violate specsSOT synch error generationSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Reference clock input	Required, Clock input = 1/10 bit rate to 700 Mbs, 1/20 above 700 MB
Minimum bit rate (high-speed mode)80 MbpsMaximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionHSDT request error generationYes, with timing control to violate specsSOT synch error generationSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Performance	
Maximum bit rate (low-power mode)10 MbpsMinimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Maximum bit rate (high-speed mode)	1.5 Gbps
Minimum bit rate (low-power mode)800 KbpsMemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionHSDT request error generationYes, with timing control to violate specsSOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Minimum bit rate (high-speed mode)	80 Mbps
MemoryUser allocated (shared among Exerciser, Analyzer and Raw Mode)Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Maximum bit rate (low-power mode)	10 Mbps
Standard1 GBOption M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsSOT synch error generationYes, with timing control to violate specsEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to violate specsProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Minimum bit rate (low-power mode)	800 Kbps
Option M04 (recommended for images)4 GBOption M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsHSDT request error generationYes, with timing control to violate specsSOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to violate specsProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Memory	User allocated (shared among Exerciser, Analyzer and Raw Mode)
Option M16 (recommended for video)16 GBPacket insertionYes, with timing control to violate specsHSDT request error generationYes, with timing control to violate specsSOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)		
Packet insertionHSDT request error generationYes, with timing control to violate specsSOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Option M04 (recommended for images)	4 GB
HSDT request error generationYes, with timing control to violate specsSOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Option M16 (recommended for video)	16 GB
SOT synch error generationNoEndof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	Packet insertion	
Endof HSDT error generationYes, with timing control to violate specsLPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)	HSDT request error generation	Yes, with timing control to violate specs
LPD transmission error generationYes, with waveform timing control and direct control of data transmitted on the linkProtocol errorsYesTurnaround error generationNo (does not operate in slave mode)		··•
Protocol errors  Yes    Turnaround error generation  No (does not operate in slave mode)		
Turnaround error generation No (does not operate in slave mode)	LPD transmission error generation	Yes, with waveform timing control and direct control of data transmitted on the link
ů – Elektrik	Protocol errors	Yes
ECC CPC error apportion Manual	Turnaround error generation	No (does not operate in slave mode)
	ECC, CRC error generation	Manual

## Keysight U4421A – Analyzer Option (602) Performance Characteristics (Continued)

Environmental specifications		
Radiated emissions (RE)	CISPR 11/EN55001	Group 1 Class A
Radiated immunity (RI)	EN/IEC 61000-4-3 frequency range @ V/m	80 MHz to 2 GHz @ 3 V/m;
		2 GHz to 2.7 GHz @1 V/m
Electrostatic discharge	(EN/IEC 61000-4-2)+ discharge air/contact (kV)	15/8
Operating temperature	Operating range: Min-max (°C)	+5 ±40
Storage temperature	Storage range: Non-operating min-max (°C)	-40 ±70
Operating humidity	max % RH @ temperature °C	80 @ 40
Storage humidity	max % RH @ temperature °C	90 @ 65
Random vibration, Operating	5 to 500 Hz random, Grms	0.21
Random vibration, Survival	5 to 500 Hz random, Grms	2.09
Half sine shock	2 mS half sine delta velocity m/sec (in/sec)	1.6 (63)
Trapezoidal shock	24 mS trapezoidal delta velocity m/sec (in/sec)	8.00 (315)
Operating altitude	(kilo feet/kilo meters)	10/3.1
Storage altitude	Non-operating (kilo feet/kilo meters)	15/4.6
Operating magnetic field immunity	A/m rms	30
Safety	IEC 61010-1	Single fault condition

## Module Configuration

	U4421A exerciser/analyzer				
Select Instrument type(s)	Analyzer only (601)	Exerciser only (602)	Exerciser + Analyzer (603)		
Select lane count	1-lane	2-lanes	4-lanes		
	(default)	(402)	(404)		
Select protocol(s)	CSI-2	DSI-1	CSI-2 + DSI-1		
	(701)	(702)	(703)		
Select memory	1 GB	4 GB	16 GB		
	(default)	(M04)	(M16)		
Select Image analysis	Image extractor (001) requires 601 or 603	Image inserter (003) requires 602 or 603			

### Chassis and Probing Configuration

### Chassis option

M9502A	2-slots	
M9505A	5-slots	

### PC control options

M9536A	Embedded PC module (no cables or adapters needed)
Connecting via PCIe® to a Desktop PC	
M9048A	PCIe desktop adapter
Y1202A	PCIe cable (x8 to x8)
Connecting via PCIe to a Laptop PC	
M9045B	ExpressCard adapter
Y1200B	PCIe cable (x1 to x8)

### Analyzer probes (with Options 601 or 603)

	REQUIRED (Logic cable)
Pick one or more of	f the following
E5381A	Flying lead adapter
E5405A	Soft touch adapter
SMA breakout to so	ft touch adapter (available from UNH-IOL)

### Exerciser probe (with Options 602 or 603)

U4422A SMA cable, MIPI D-PHY, 13 leads/1.5 Gbps
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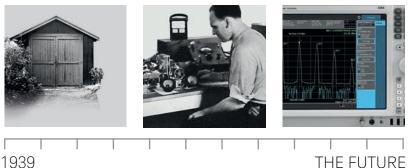
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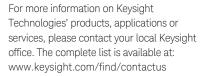
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